Toronto Wireline Workshop
High-Density Optical Links

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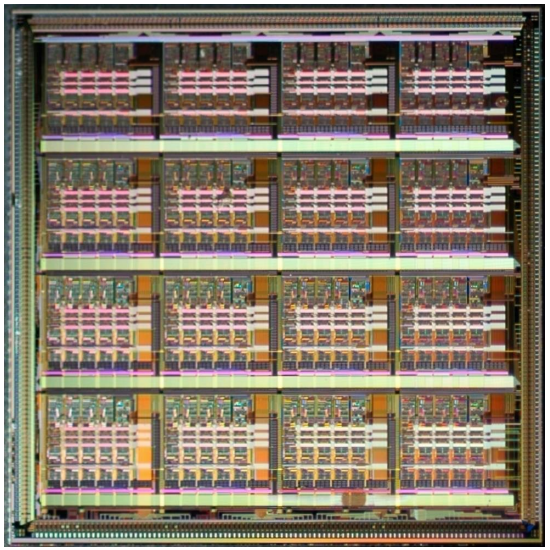
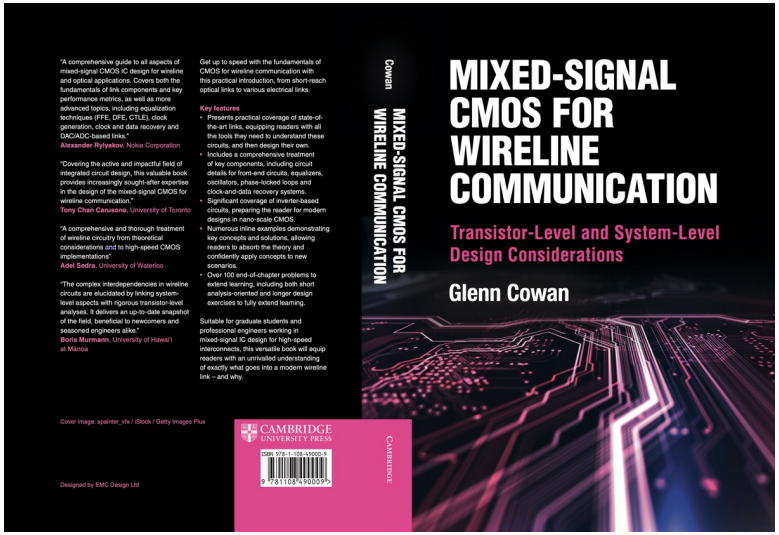
High-Level Outline

- Professional trajectory
- Research group at Concordia
- Solving the energy problem of I/O

Professional Trajectory

- **BASc (1999), EE, UW**
- **MS + PhD (2005), EE, Columbia**
  - VLSI Analog Computer, 100 mm^2
- **2005-2007: IBM Watson**
  - VCO/PLL design
  - Circuits to explore process variation
- **2007–: Concordia University**
  - SSCS chapter chair since 2019
  - 2024 book release
  - IC design for high-speed and other applications

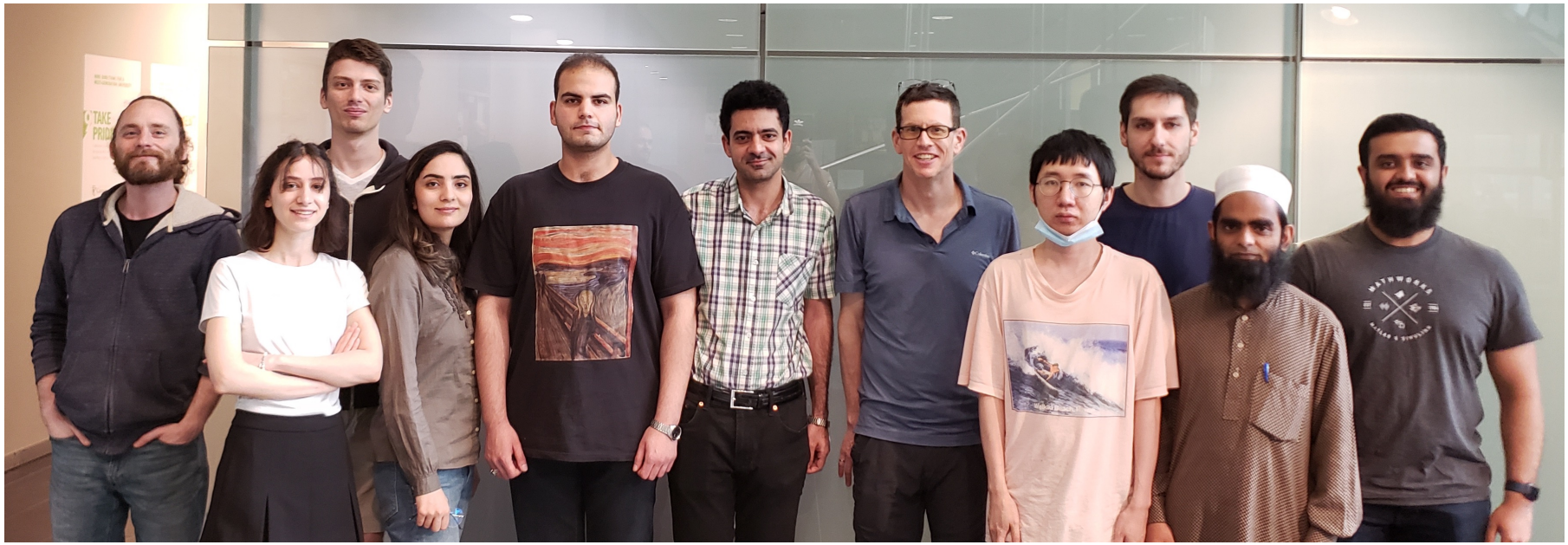




Research Directions

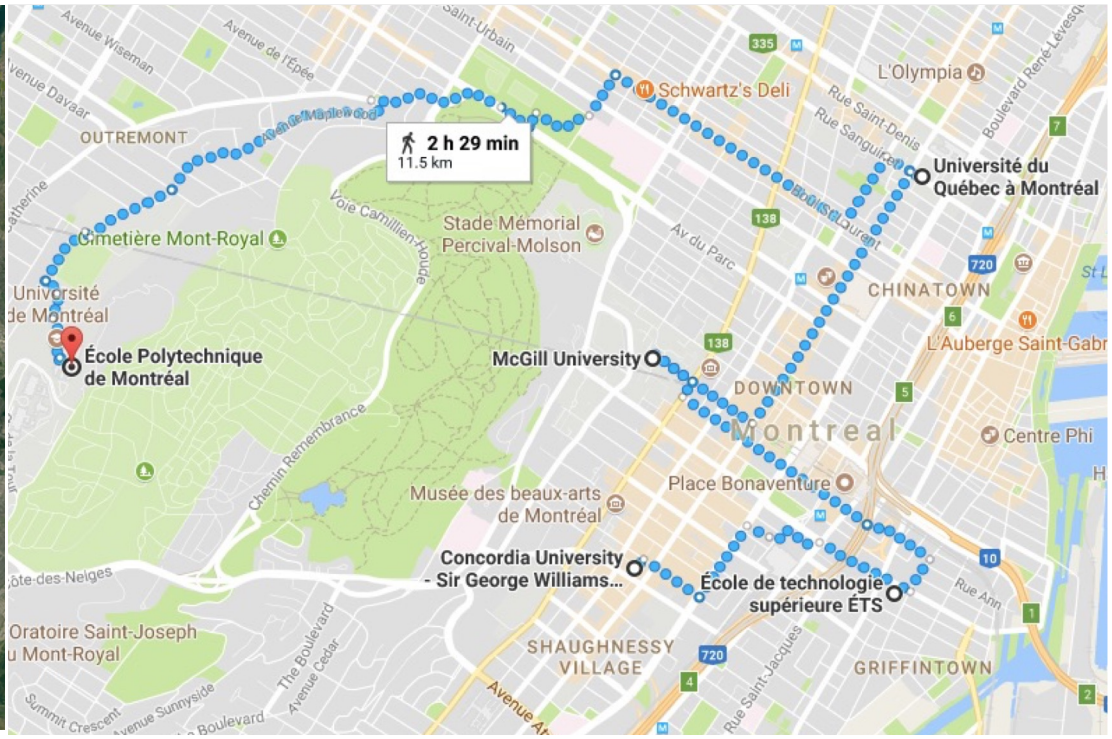
- **ICs for wireline**
  - Oscillators, PLLs, CDRs, photodiodes, optical receivers, laser diode drivers, ring-modulator drivers, thermal control
- **Systems in package for harsh environments**
  - MEMS actuators, gate drivers, class-D amplifier control, PGAs
- **Contactless ECG measurement**
  - Automatic bandwidth control, motion artifact modelling and mitigation
- **Mixed-signal computation and security**
  - Spiking neural networks, physical unclonable functions, ODEs

Research Team



- Absent: James Kyriacou (MASc), Sara Granata (MASc), Thimoté Desroches (MASc, ETS), Thin Tran (MASc, ETS), Benoit Malenfant (MASc, ETS)
- Recent grads: Nurahmed Aimaier (PhD, Dolphin), Allan Riboullet (MASc, ETS → in France), Sara Radfar (MASc, Linear optical receivers, Axonal Networks), Ata Mahsafar (MASc, CMOS for Optical logic gates)

Montreal: A City of Universities



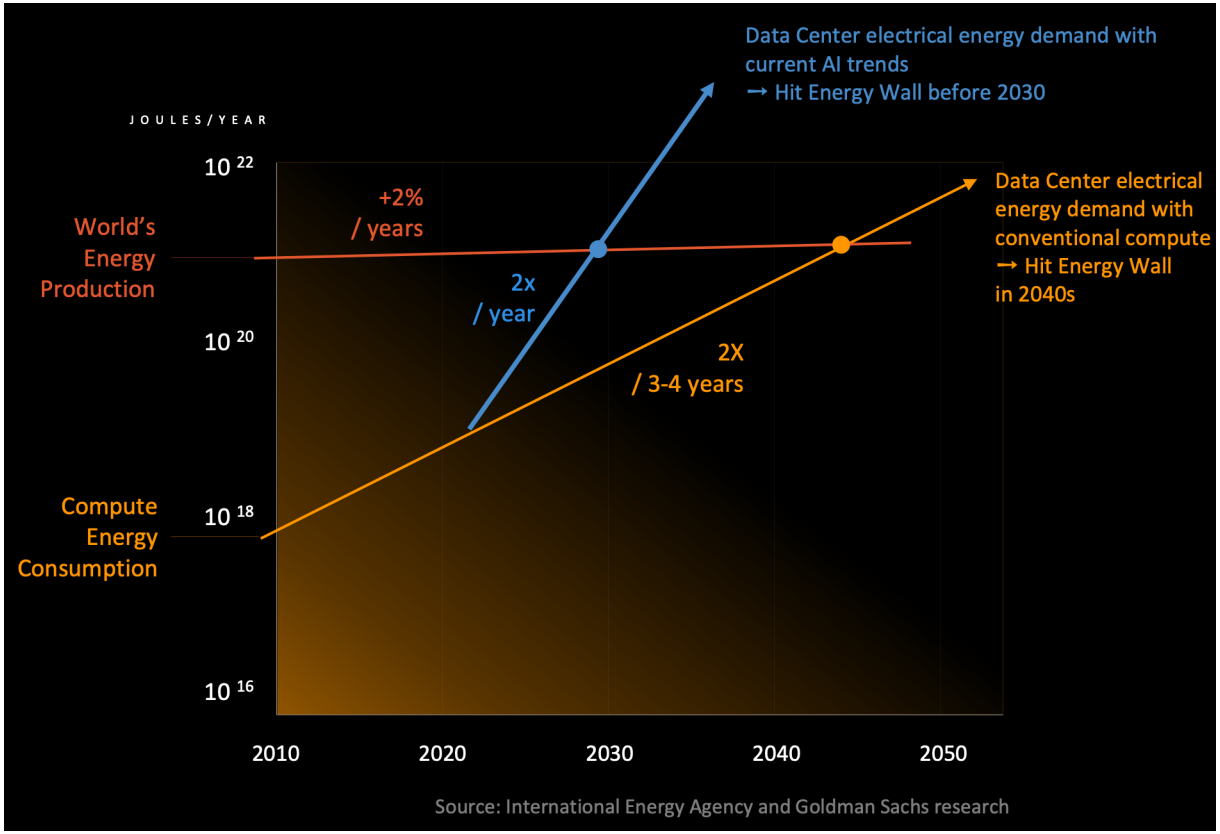
- When will you visit next?

Outline

- **Problem context**
- **Metrics**
- **Recent trends**
- **Potential directions**
  - Non-retimed, but not necessarily linear
  - Dense electrical to WDM
  - CPOs w/o EIC
- **Conclusions**

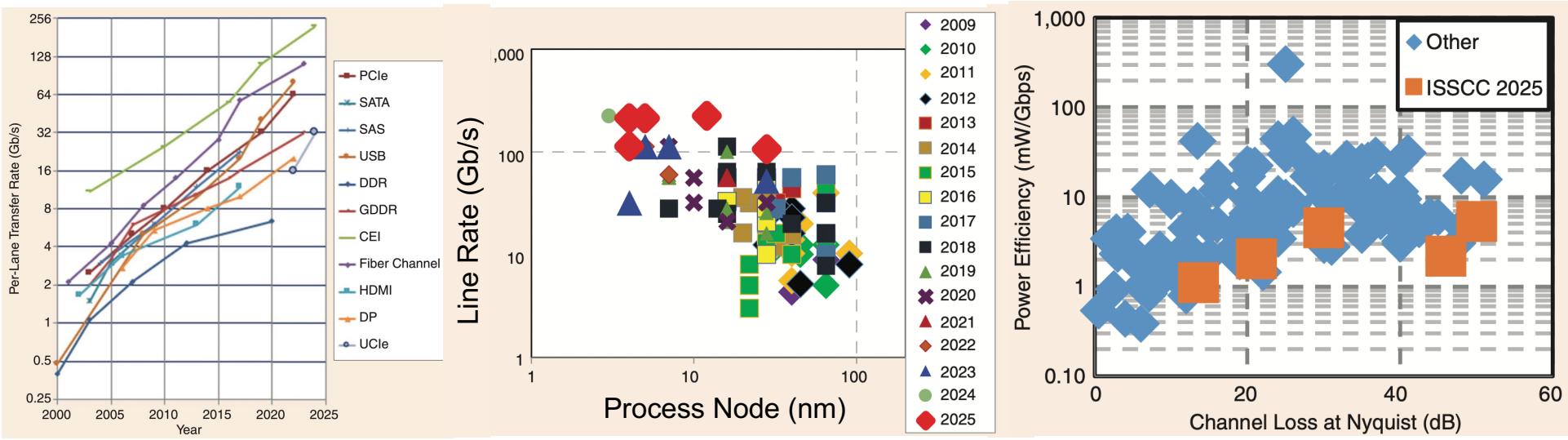
Energy Trends

- Compute energy
- Faster now: AI
- Production is flat



MediaTek, ISSCC 2026

Per-Lane Metrics

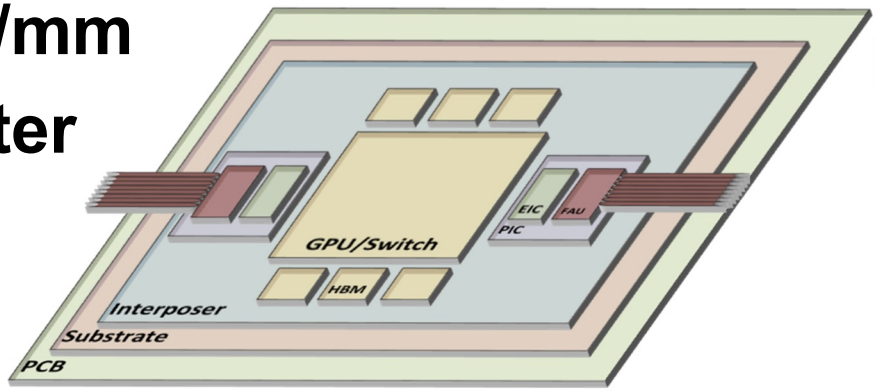


SSCS Magazine 2025

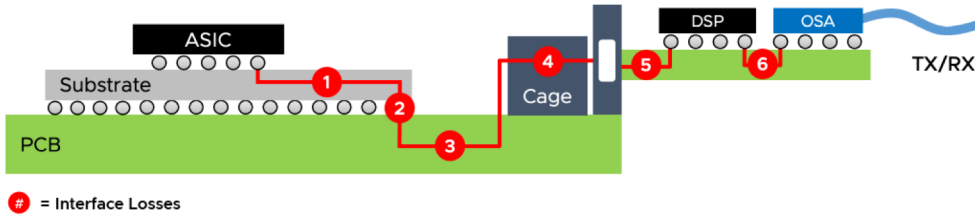
- **Data rate**
- **Energy per bit (pJ/bit)**

Aggregate Data Rate Metrics

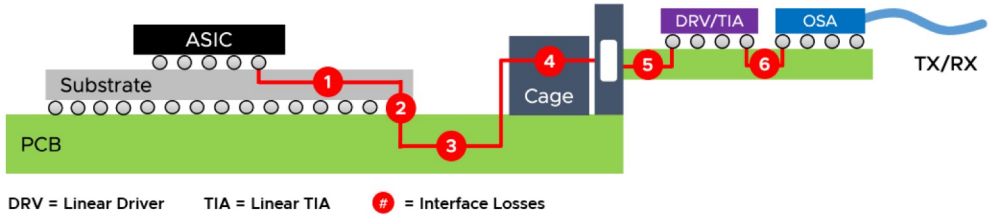
- Beachfront/shoreline: Tb/s/mm
- Distance increases perimeter
- Area density: Tb/s/mm^2
- Cost and vertical coupling



Optical Transceiver Architectures: Pluggable



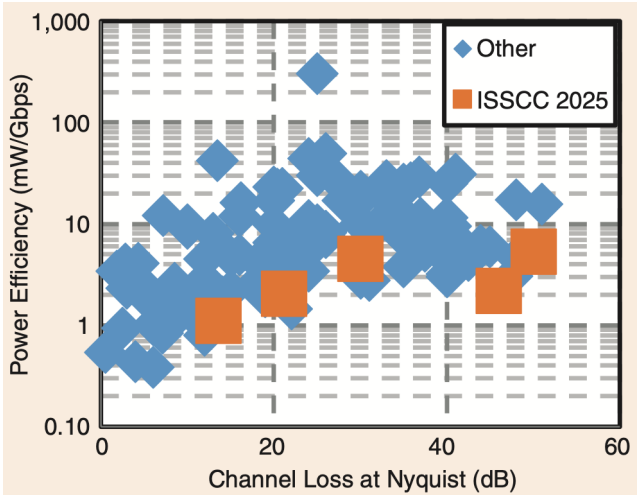
DSP pluggable optical module



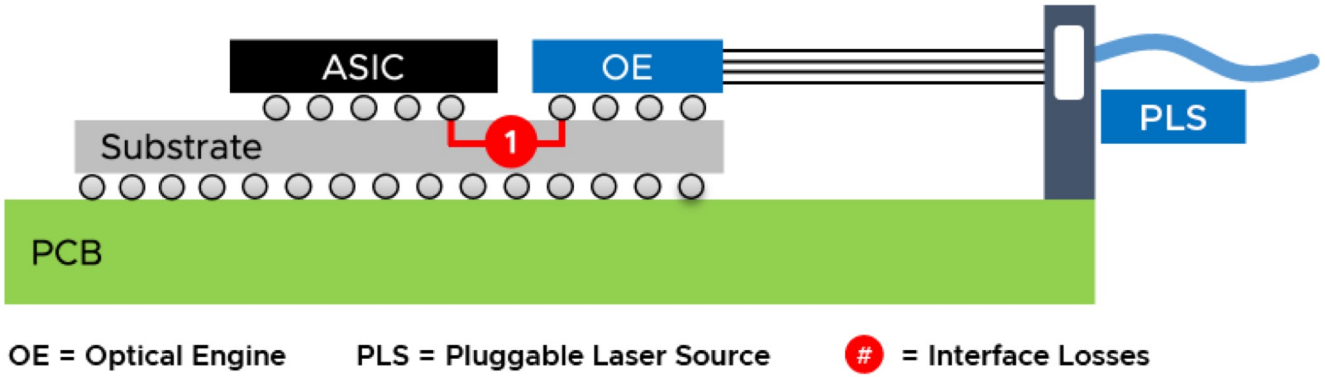
Linear pluggable optical module

ISSCC 2026, Broadcom

- **Pluggable is serviceable**
- **Interface losses = energy dissipation**
- **Linear pluggable, DSP: TRx to Host**
- **Linearity needed for residual ISI**



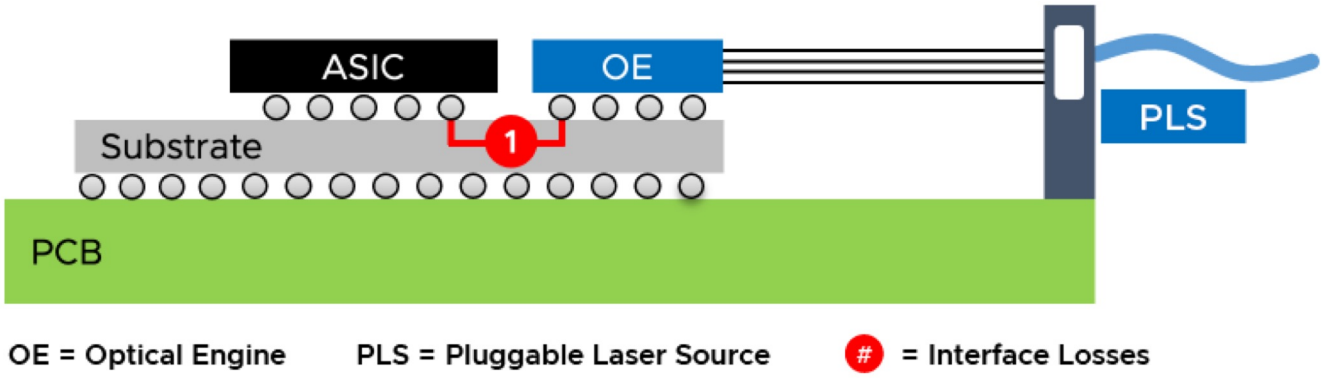
Optical Transceiver Architectures: CPOs



- **Co-packaged optics: Shorter traces, less loss**
- **Less serviceable → Pluggable light sources**
- **Much easier to get bits to and from OE**
  - Less loss and denser I/O
  - May eliminate retiming in OE on one or both ends

ISSCC 2026, Broadcom

Optical Transceiver Architectures: CPOs

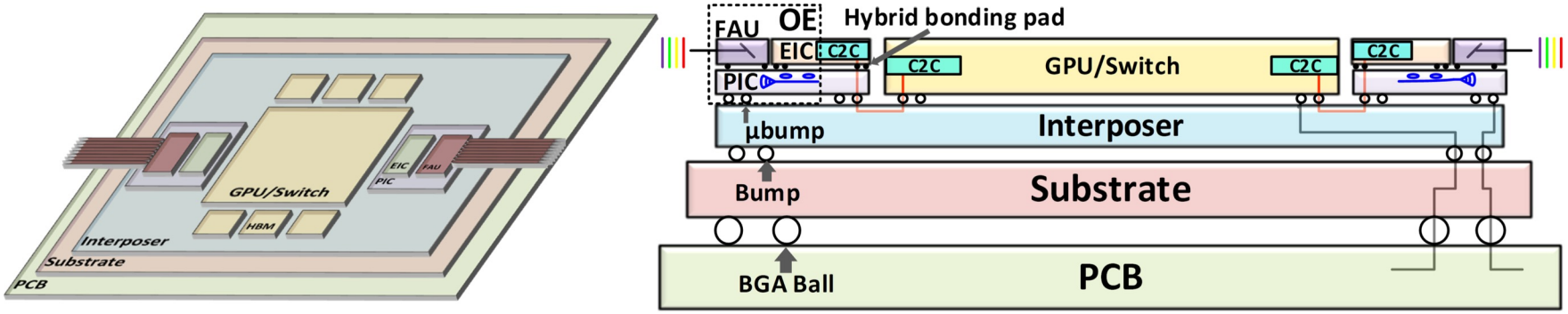


- Broadcom solution: 106 Gb/s PAM4, MZM
- Retimed on OTx, direct drive for ORx
- 7 nm CMOS stacked on PIC
- 4.2 pJ/bit

ISSCC 2026, Broadcom

Detailed CPO Cross-Sectional View

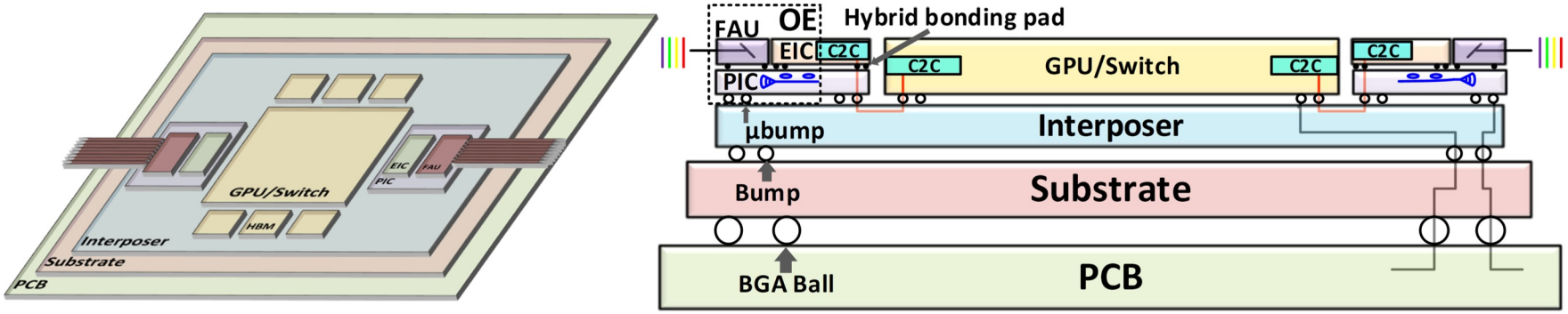
ISSCC 2026, NVIDIA



- Short, dense chip-to-chip links (C2C) @ 32 Gb/s
- 2.6 pJ/bit, incl laser (10 % WPE)
- Wavelength division multiplexing gives 256 Gb/s/fibre
- Efficient due to modest line rate and short links

Detailed CPO Cross-Sectional View

ISSCC 2026, NVIDIA



- Forwarded clock, retiming in ORx
- Test chip has mux/demux for testing
- EIC between GPU and PIC

XSR Performance Comparison

	Yousry ISSCC 2021 (MediaTek)	Shivnaraine ISSCC 2021 (Rambus)	Poon VLSI 2021 (Xilinx)	Gangasani VLSI 2024 (Marvell)
Technology Node	7nm	7nm	7nm	5nm
Data Rate	112G PAM4	106.25G PAM4	112G PAM4	113G PAM4
Lanes	8 Tx / 8 Rx	8 Tx / 8 Rx	8 Tx / 8 Rx	8 Tx / 8 Rx
Beachfront Density	N/A	722 Gbps/mm	870 Gbps/mm	606 Gbps/mm
Reach	50 mm	50 mm	20 mm	80 mm
Power Efficiency	1.7 pJ/bit	1.55 pJ/bit	1.24 pJ/bit	1.1 pJ/bit
TX equalization (driver type)	5b DAC w/ 5-tap FFE in DSP (SST)	3-tap LUT FFE w/ 5b DAC (SST)	2-tap FFE (SST)	3-tap FFE (SST)
TX output swing	0.6 V_{ppd}	0.9 V_{ppd}	0.9 V_{ppd}	N/A (>0.65 V_{ppd})
RX equalization (boost)	CTLE (8dB)	CTLE (N/A)	CTLE (5dB)	CTLE (5dB)

Dickson DL Talk 2025

UCI Performance Comparison

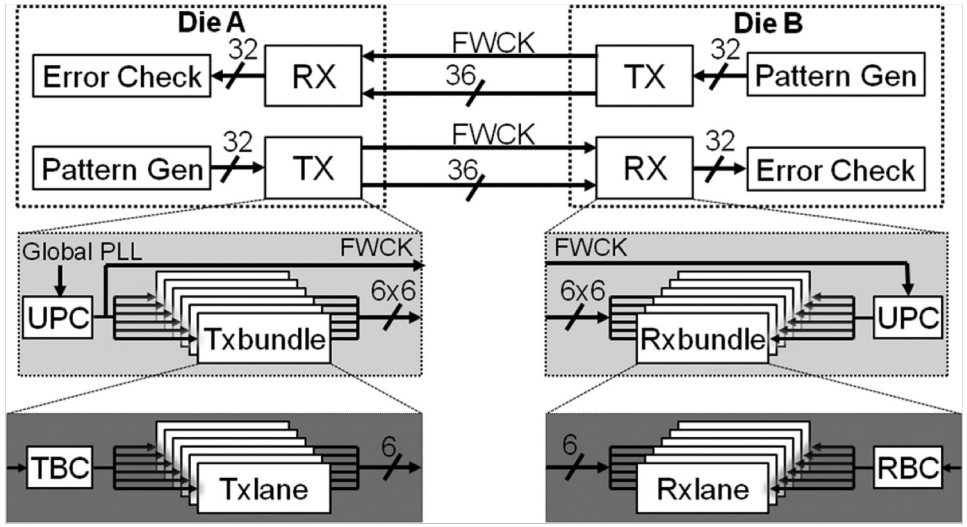
Dickson DL Talk 2025

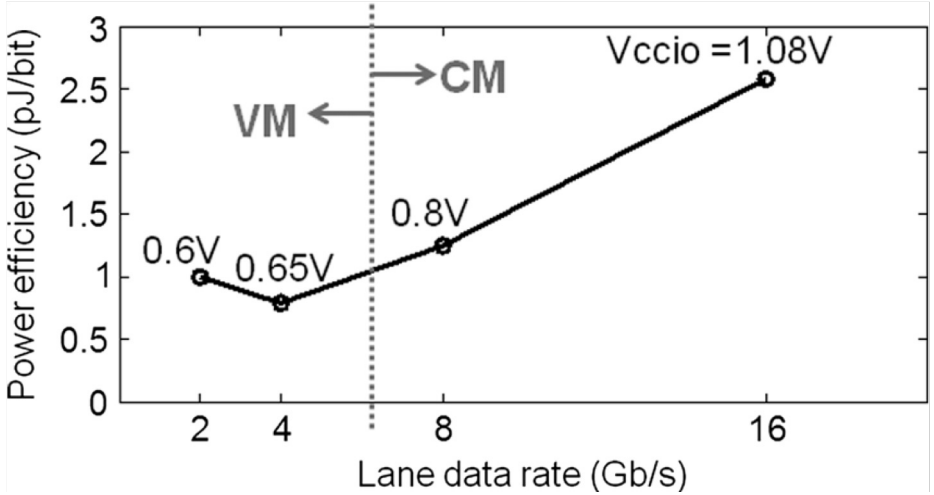
	UCIe Specification	Turker Melek ISSCC 2025 (Cadence)	Lin ISSCC 2025 (TSMC / AMD)
Technology Node		3nm	3nm
Standard	UCIe	UCIe	UCIe
Bus Width (per module)	16, 32, 64	64	64
Data Rate (per wire)	4 to 32 Gb/s	16 Gb/s	32 Gb/s
Signaling	Single-ended NRZ	Single-ended NRZ	Single-ended NRZ
Bump Pitch		45 µm	45 µm
Reach	< 2mm	1.4 mm	1.7 mm
Packaging	Advanced Package	Silicon interposer (CoWoS)	(1) Silicon bridge (2) Organic interposer
Clocking Architecture	Half-rate (≤ 16Gb/s) Half OR quarter-rate (≥ 24 Gb/s)	Half-rate TX & RX	Quarter-rate TX & RX
Energy Efficiency		0.29 pJ/bit	0.6 pJ/bit
Shoreline	388.8 µm	388.8 µm	388.8 µm
Shoreline Density	up to 10.5 Tbps/mm	5.27 Tbps / mm	10.5 Tbps / mm

Proprietary Links

	UCIe Specification	Seong ISSCC 2023 (Samsung)	Nishi VLSI 2022 (NVidia)	Nishi VLSI 2023 (NVidia)
Technology Node		4nm	5nm	5nm
Standard	UCIe	Proprietary	Proprietary	Proprietary
Bus Width (per module)	16, 32, 64	39	19	19
Data Rate (per wire)	4 to 32 Gb/s	32 Gb/s	50.4 Gb/s	25.2 Gb/s
Signaling	Single-ended NRZ	Single-ended NRZ	Simultaneous Bi-directional	Single-ended NRZ
Bump Pitch		50 µm	55 µm	55 µm
Reach	< 2mm	1.4 mm	1.2 mm	1.2 mm
Packaging	Advanced Package	Silicon interposer	On-chip replica channel	On-chip replica channel
Clocking Architecture	Half-rate (≤ 16Gb/s) Half OR quarter-rate (≥ 24 Gb/s)	Quarter-rate	Half-rate	Half-rate
Energy Efficiency		0.44 pJ/bit	0.297 pJ/bit	0.19 pJ/bit
Shoreline	388.8 µm	250 µm	330 µm	330 µm
Shoreline Density	up to 10.5 Tbps/mm	8 Tbps / mm	N/A (11.0 Tbps/mm)	N/A (5.8 Tbps/mm)

Case for Modest Data Rate





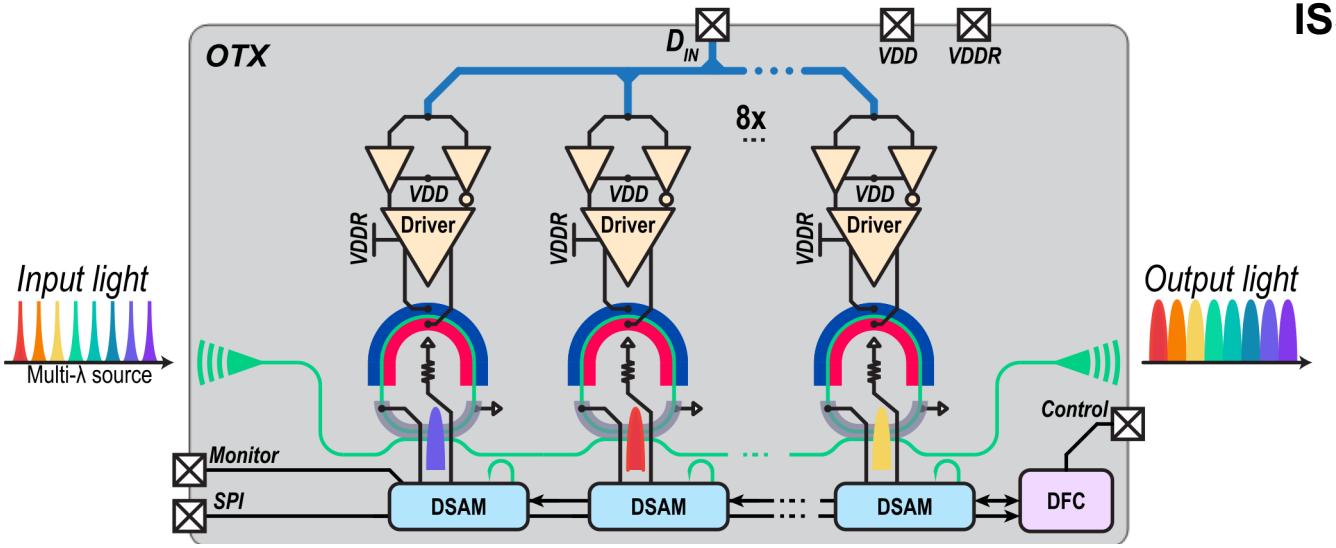
- 50 cm twinax cable
- Clock forwarding
- 32 nm CMOS

- Power increases with DR
- Energy/bit increases

JSSC 2013, Intel

Efficient Optical Tx

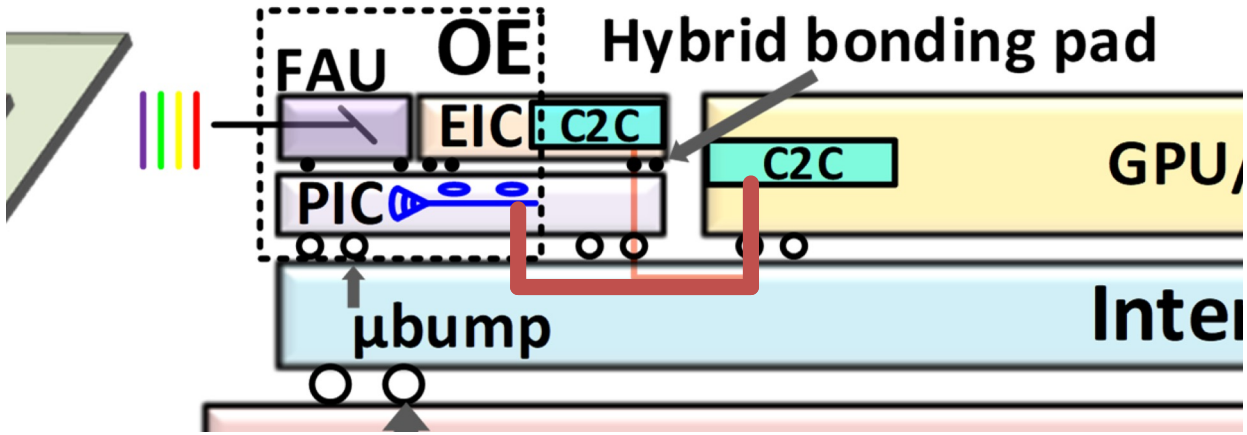
ISSCC 2026, UPenn



- 8 x 38 Gb/s, WDM, monolithic integration
- Driver efficiency ~106 fJ/bit
- 8 dBm per λ @ 10% WPE adds 1.6 pJ/bit

Direct Connect: Switch to PIC

ISSCC 2026, NVIDIA



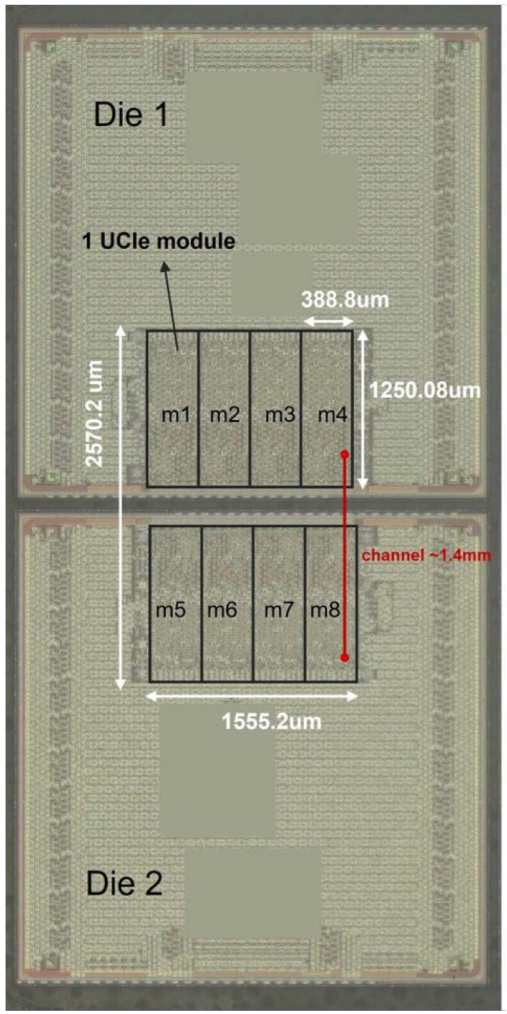
- As reach shrinks, connect PIC directly to Host?
- Can we tolerate the distance?
- What is the minimum distance?
- Advocates of chiplets: Almost as good as on-die

UCIe Channel Dimensions

- UCIe module: 64 lanes Tx & Rx
- ~ 1 mm, 7 ps TOF
- 0.29 pJ/bit @ 16 Gb/s (SE)

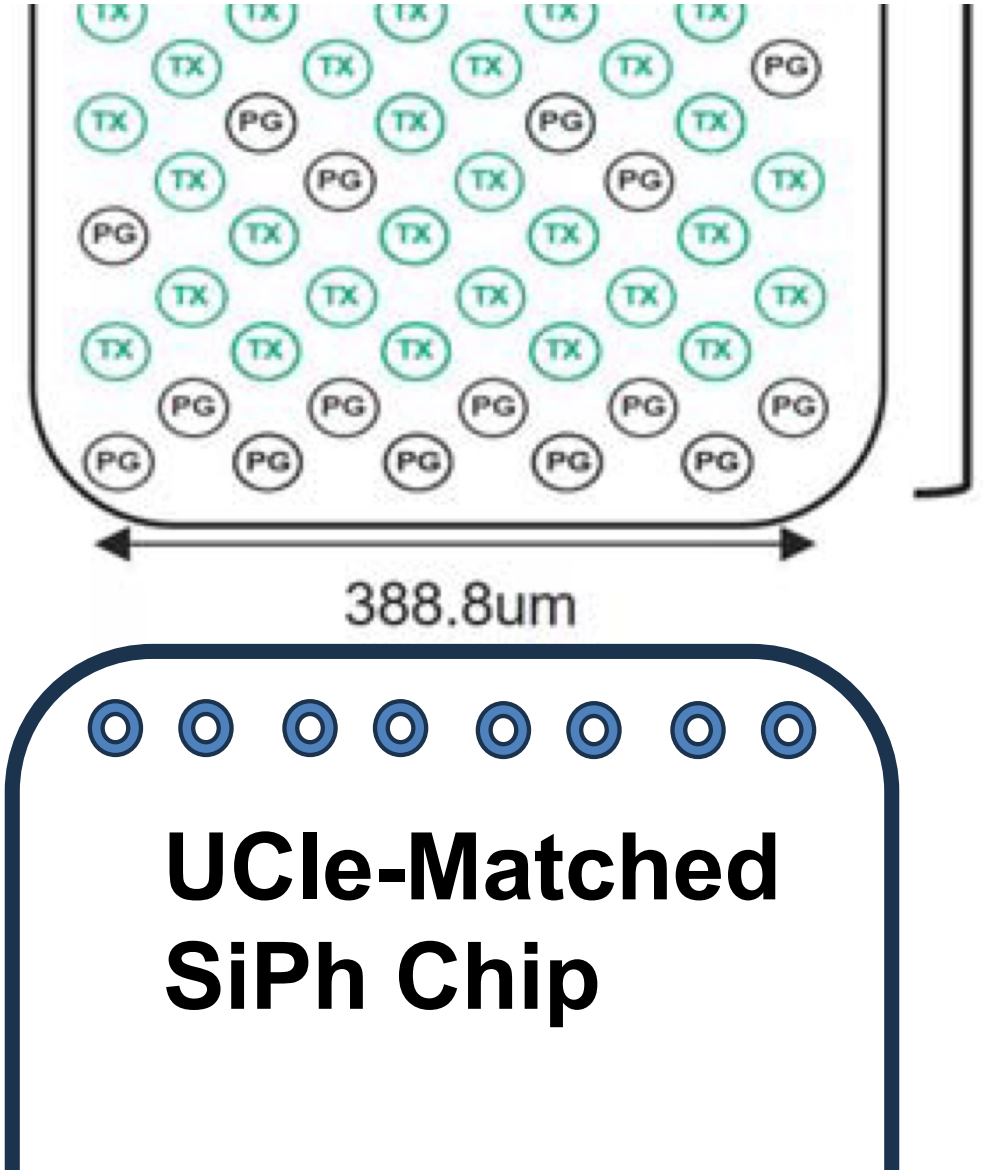
ISSCC 2025, Cadence

Chip edge



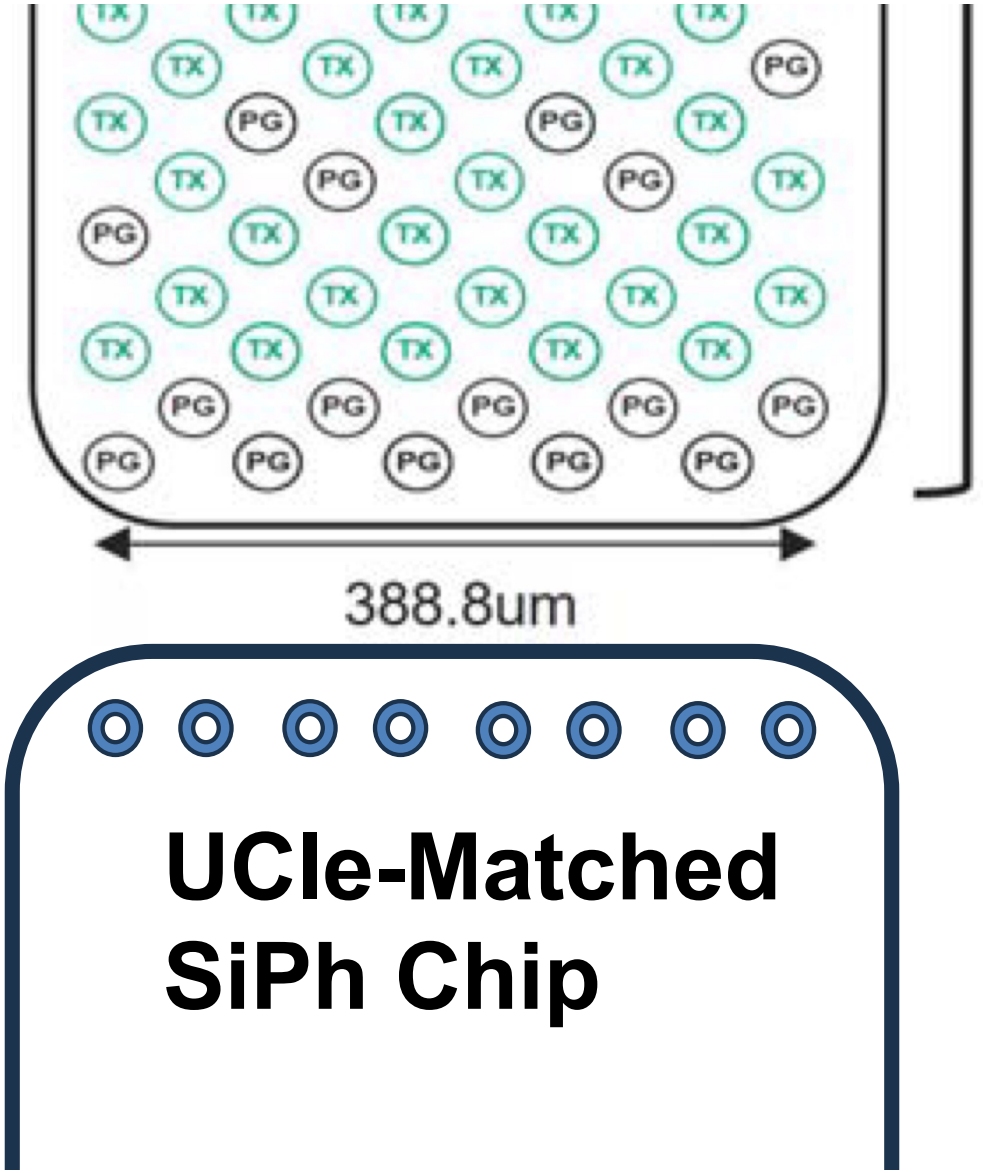
UCIe-Sized Optical Tx

- **Pads ~ ring diameter**
- **Need ring tuning pins**
- **Differential drive**
  - > VDD swing needed
  - Modest rate = higher Q
- **Increase depth**
- **Separate UCIe for Rx**



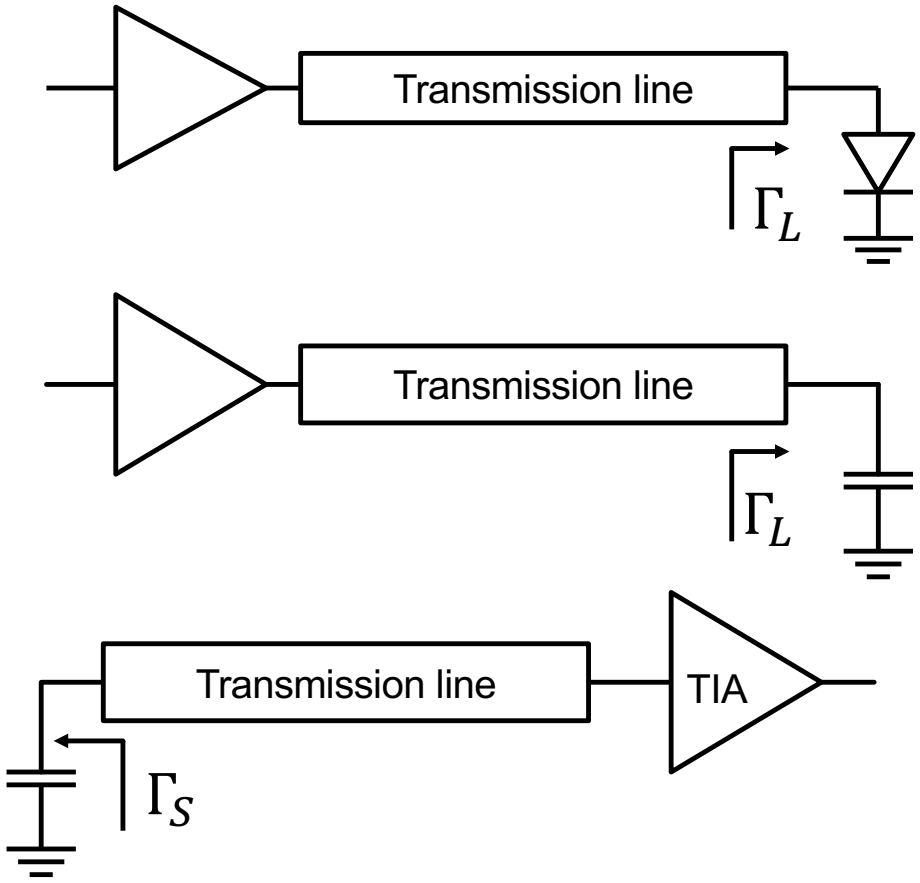
Challenges

- **Driving cap via TL**
- **PD to TIA via TL**
- **I/O count per lane**
  - Differential ring and TIA
  - Tuning for ring



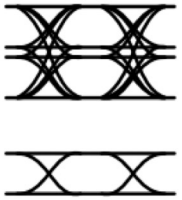
Ring/PD Via Transmission Line

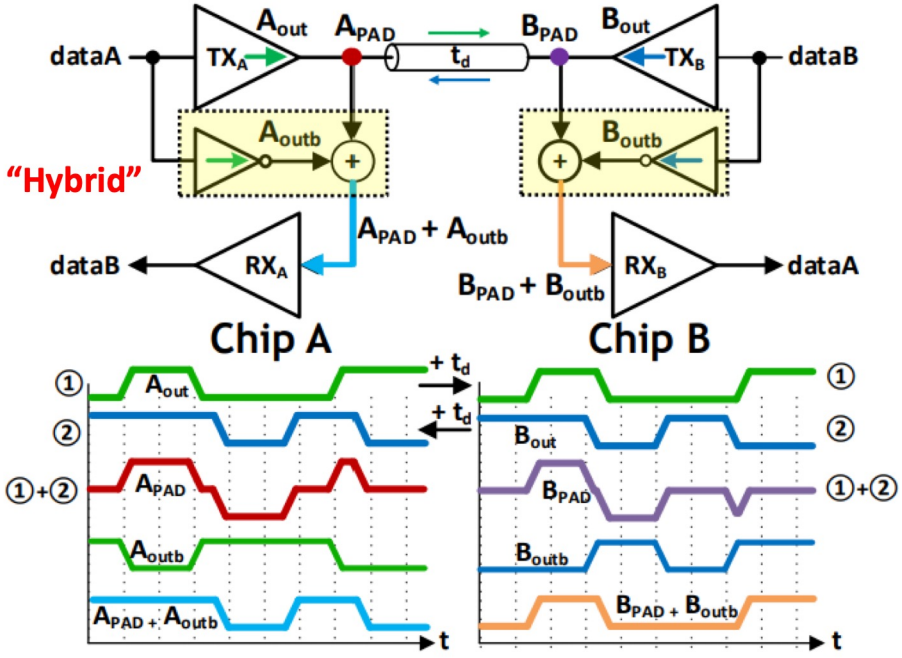
- **TL between driver/VCSEL**
  - Can be matched: $\Gamma_L < 1$
- **Driving ring via TL**
  - $\Gamma_L = 1$
  - Add termination across ring?
- **PD to TIA via TL**
  - $\Gamma_S = 1$
- **Power/termination**



Simultaneous Bidirectional Signaling

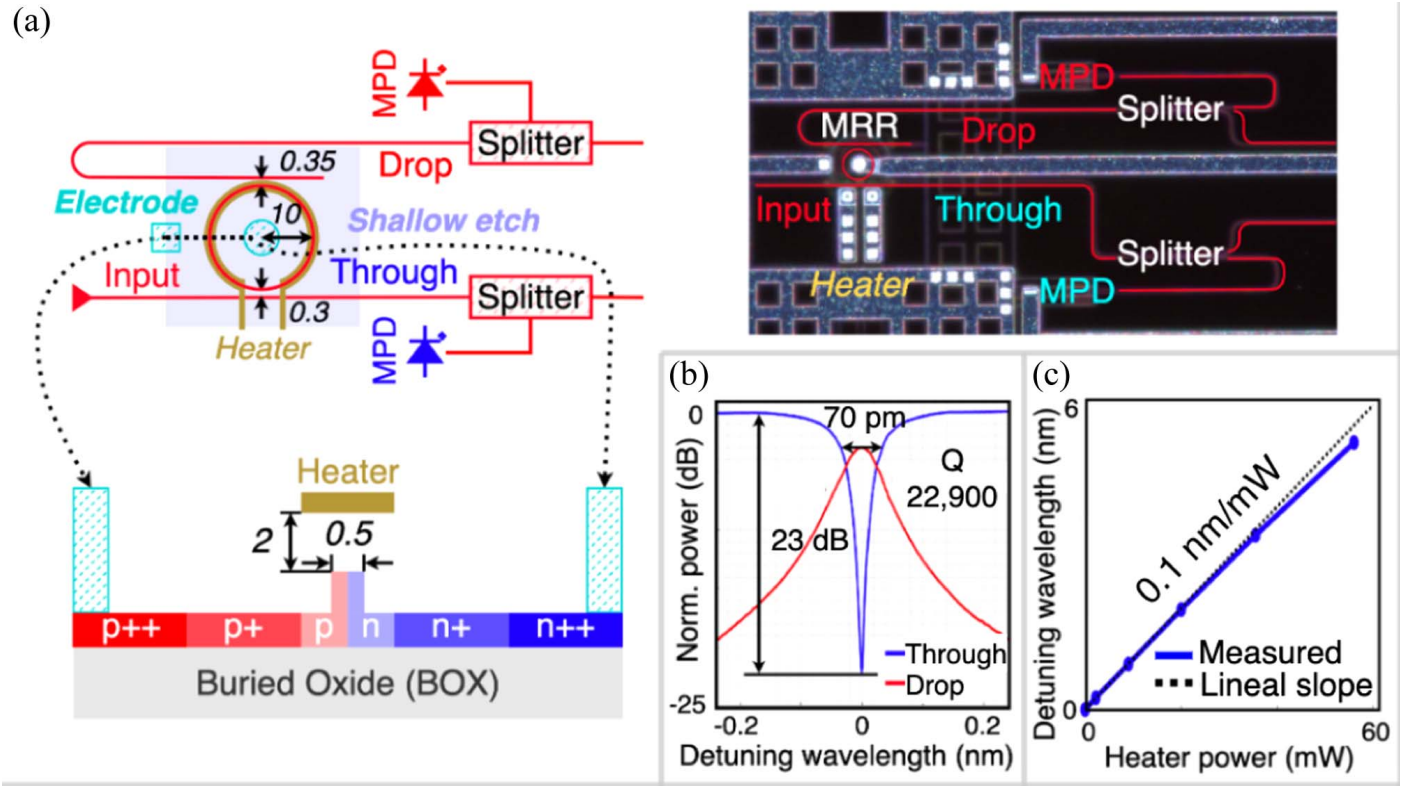
- Rx tolerant to uncorrelated interference
- View reflection through same lens and EQ
- Observation ≠ actuation
- Short TOF (< 1 UI)
- Low loss (many reflections)





VLSI 2022, NVIDIA

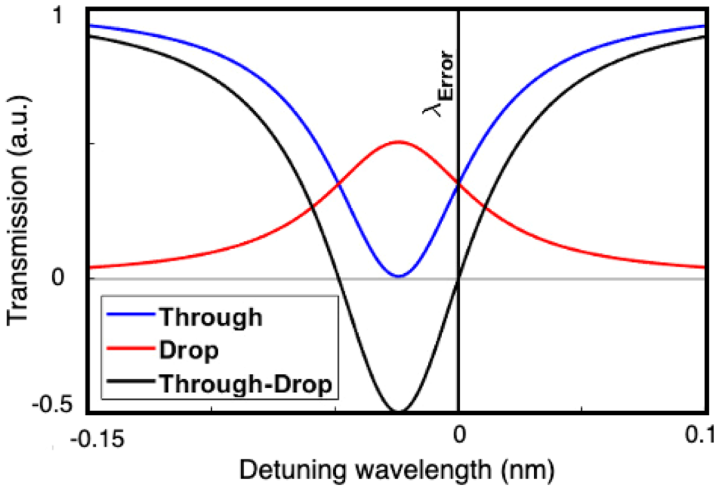
Our Approach to Ring Tuning

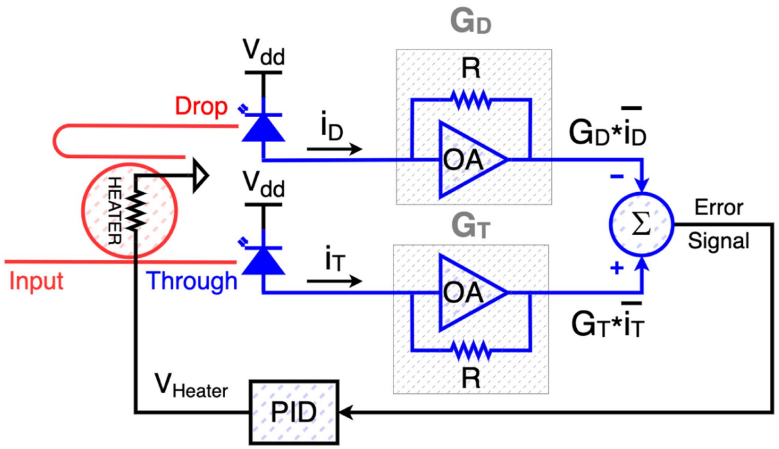


JLT 2025

- Double bus ring: Quasi complementarity of outputs

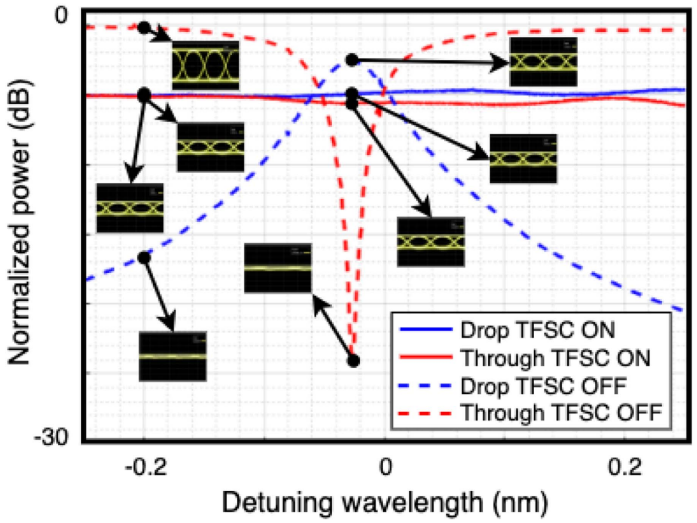
Reference & Calibration Free Lock Point

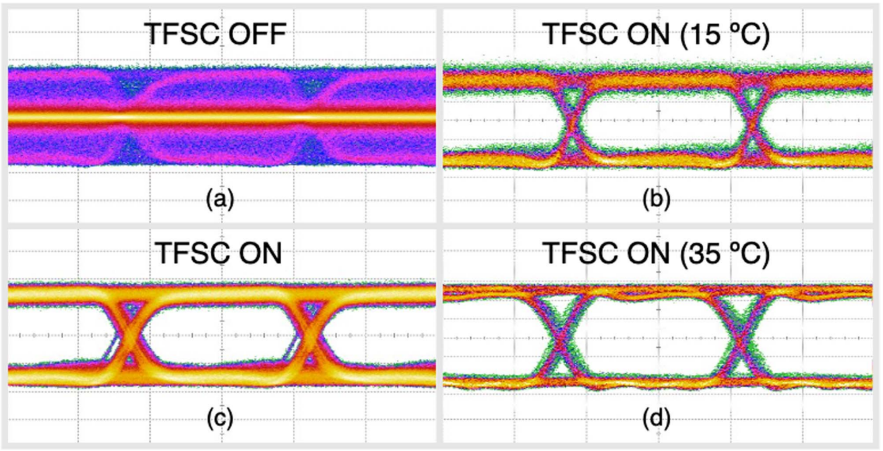




- Lock at high slope for max OMA
- Difference between through and drop → Error signal
- PI control
- Thermal Feedback Stabilization Circuit (TFSC)

Reference & Calibration Free Lock Point





- Locks ring over wide temperature sweep
- L: Wavelength sweep
- R: Temperature sweep
- Robust to temperature, wavelength, input power

Summary

- **Shorten the electrical traces best performance**
- **Selective use of equalization**
- **Leverage C2C density, WDM → Modest rate**
- **Eliminate EIC in CPOs**
  - Solve challenges of TLs
- **Use simple thermal tuning**

References

- S. Mirabbasi and L. C. Fujino, "Through the Looking Glass—The 2025 Edition: Trends in solid-state circuits from ISSCC," in *IEEE Solid-State Circuits Magazine*, vol. 17, no. 1, pp. 97-118, winter 2025
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- J. G. Echeverría *et al*., "Self-Calibrated Microring Weight Function for Neuromorphic Optical Computing," in *Journal of Lightwave Technology*, vol. 43, no. 2, pp. 602-610, 15 Jan.15, 2025

CONCORDIA

Questions?

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