Reliability of Printed Circuit Boards for Critical Applications

Professor Tan Cher Ming
Director, **reliability sciences and technologies**, Taiwan
Professor, Department of electronic engineering, and Institute of radiation research, Chang gung university, Taiwan
Distinguished Professor, Department of mechanical engineering, Ming chi university of technology, Taiwan
IEEE distinguished lecturer of electronic devices society
Editor, IEEE transaction on device and materials reliability; Series Editor of Springbrief on Reliability
Advisory Panel of Elsevier Publisher and Applied Physics Letters (Electronic Devices)
Top 2% Scientists in the World (2021-2025) @Stanford University
Top 0.05% Scientists in Semiconductor Reliability (2025 – within top 30) @ScholarGPS
Ishikawa-kano quality awardee of 2014, individual category
Fellow of Singapore quality institute; Fellow of institute of engineer, Singapore; Fellow of IAAM, Sweden
Senior member of IEEE and American society of quality (ASQ);

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Success will not come by accident with today's complexity, but requires balanced design, expert and quality build, and rigorous evaluation based on the best available knowledge of today's failure mechanisms.

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Impact of PCB Design on Component Reliability

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List of Allowable value of components surface temperature

Components	Allowable Surface Temperature/°C	Components	Allowable Surface Temperature/°C
Transformer, choke	95	Ceramic capacitor	80-85
Metal film resistor	100	Glass ceramic capacitor	200
Carbon-film resistor	120	Silicon transistor	150-200
Palladium-film resistor	200	Germanium transistor	70-90
Pressed wire wound resistor	150	Vacuum tube	15-200
Printed resistor	85	CMOS fully sealed flat package	125
Painting wire wound resistor	225	Ceramic DIP, black porcelain DIP	
Paper capacitor	75-85	CMOS plastic DIP	85
Film capacitor	60-130	TTL small-scale IC	25-125
Mica capacitor	70-120	TTL middle-scale IC	70-85

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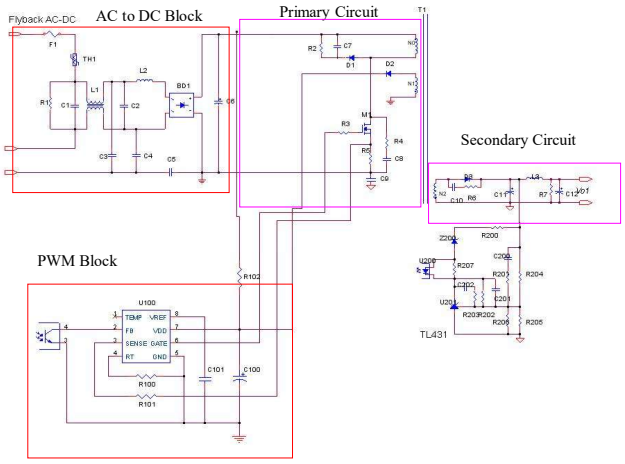
FLYBACK CONVERTER



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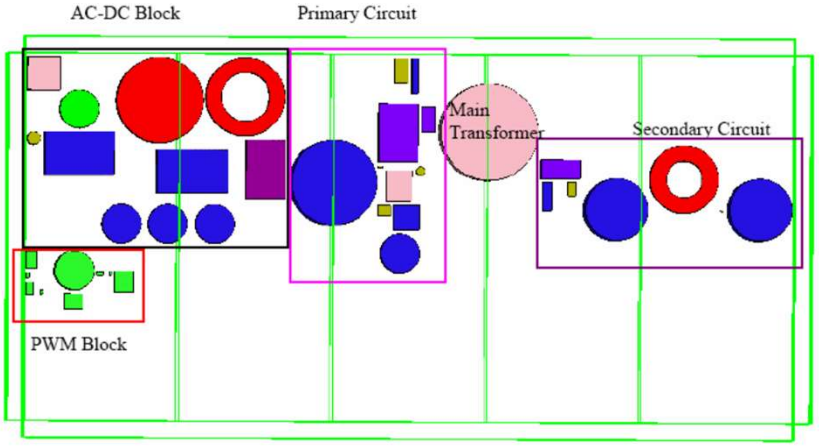
LAYOUT IN ICEPAK (TOP VIEW)



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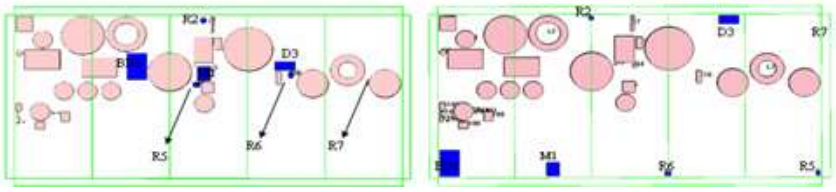
DEFAULT CASE VS. BETTER CASE (PLACEMENT)



Components	Power Lost (Watts)			
	User Input	Worst Case	Better Case	Difference
BD1	0.7835	0.7311	0.6871	0.044
D3	2.183	1.586	1.762	-0.176
M1	0.9595	0.7168	0.7585	-0.0417
R2	0.5371	0.5286	0.489	0.0396
R5	0.242	0.2414	0.2312	0.0102
R6	0.07395	0.07386	0.07151	0.00235
R7	0.05	0.05001	0.05001	0

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SIMULATION RESULTS

Ref.	Worst Case (°C)	Better Case (°C)	Temperature Difference (Worst – Better) °C	% Difference
R7	594	589.2	4.8	0.81
R5	404.7	344	60.7	15.00
R2	403.9	354.4	49.5	12.26
D3	376.5	233.5	143	37.98
M1	300.8	282.2	18.6	6.18
R6	254.4	125.5	128.9	50.67
BD1	127.1	95.5	31.6	24.86

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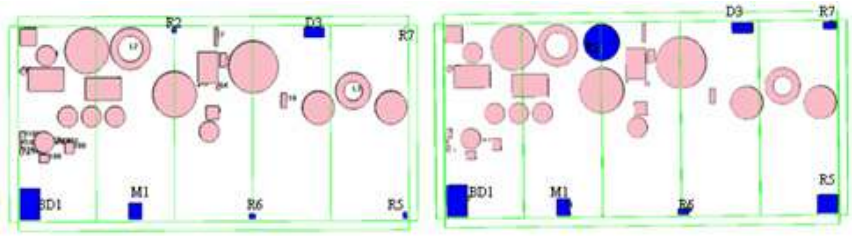
BETTER CASE VS. BEST CASE (SIZE INCREMENT)



Components	Power Lost (Watts)			
	User Input	Better Case	Best Case	Difference
R2	0.5371	0.489	0.4844	0.0046
R5	0.242	0.2312	0.2363	-0.0051
R6	0.07395	0.07151	0.07353	-0.00202
R7	0.05	0.05001	0.04405	0.00596

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SIMULATION RESULTS

Ref.	Better Case (°C)	Best Case (Size) (°C)	Temperature Difference (Better – Best(Size)) (°C)	Difference (%)
R7	589.2	37.86	551.34	93.57
R2	354.4	63.85	290.55	81.98
R5	344	52.05	291.95	84.87
R6	125.5	55.88	69.62	55.47

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PCB Layout and Reliability

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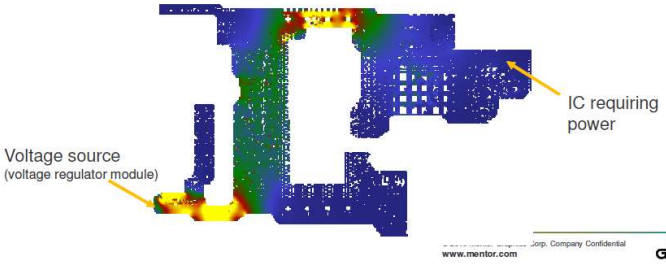
System-Level Power Optimization
Trading-off Cost and Performance

- IC design for low power is driving need for complex Power Distribution Networks (PDNs)
  - Multiple voltage rails to supply lower voltages and tolerances
  - Increased current requirements
- Downstream impact on PCB/system design
  - More power distribution networks (PDNs)
  - CAD Designer must create complex area fills



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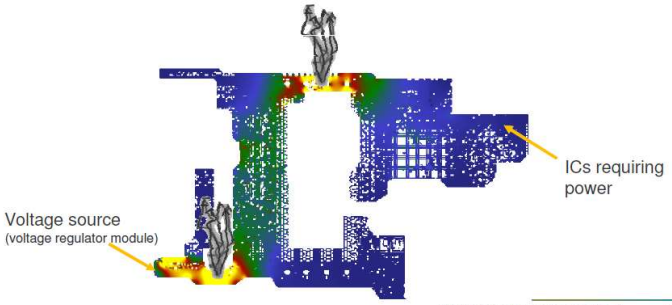
High Current Densities in Power Distribution Networks

- Common problems:
  - — High current densities in plane neck-downs and vias
  - — Leads to dielectric or via breakdown, board failure, fires
  - — Causes increase in PCB and System heat dissipation



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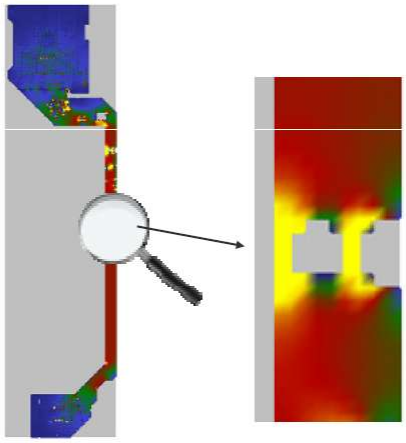
Real World Customer Example

- Analysis of a power rail shows cut-outs that create a current density problem.



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Component placement & PCB reliability

Component placement on opposite sides of a PCB can increase or decrease its flexibility.

Identical components placed on opposite sides of the PCB result in localized stiffening that makes the board appear infinitely stiff, reducing thermal cycling lifetime.

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Overview of Different type of PCB Reliability Issues for SMT and Lead Free Solders

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Introduction

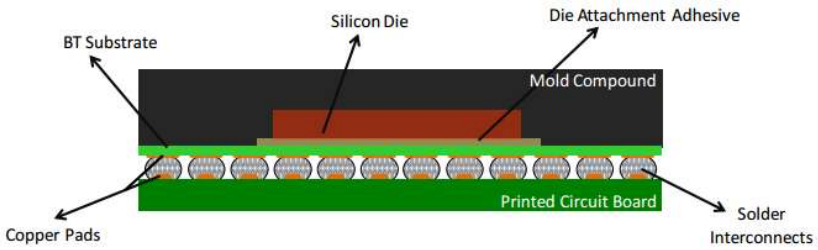

Figure 1.5 : Typical Ball Grid Array (BGA) electronic package architecture

Table 1.1 Thermal and mechanical properties of various packaging materials

Material	Elastic Modulus (E) (GPA)	Coefficient of Thermal Expansion (CTE) (10^{-6} 1/K)
Mold Compound	23.5	15
Silicon Die	162.7	2.5
Die Attach Adhesive	6.8	52
BT Substrate	18	12.4
Solder Balls	30.5	24.5
Printed Circuit Board	17	14.5

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Introduction

- The main reliability concerns associated with electronic components are associated with the following causes:
  1. Thermally Induced stresses due to exposure to high operating temperatures
  2. Mechanically Induced stresses due to careless handling-drop; and operation in vibrating environment.
  3. Residual stresses from manufacturing processes
  4. Electro-migration, Transient static discharge and other electrically induced failures
- With regard to the mechanical failures, especially those caused due to thermally or mechanically induced stresses, the interconnects between various levels of a component are rendered most vulnerable to failure.
- Furthermore, since they form a very significant part of a component, their failure can result in drastic failure of the whole component.

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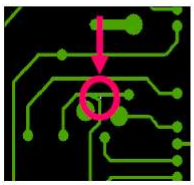
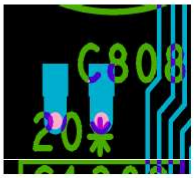
Design Issues which Affect Reliability

Fabrication Examples

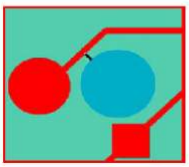
Acute angles create acid traps. While these may not cause failure at test, the acid continues to etch even after lamination, weakening the circuit.

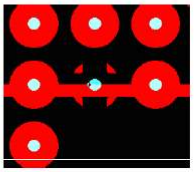




Silkscreen on pads will create problems with solder quality which may not manifest as a problem until it is put into use.

Non-plated thru holes too close to copper puts stress on the prepreg, causing a possible fracture in the circuit.





Starved thermal vias prevent proper heat containment and may effect quality of hole plating, resulting in a potential cracked barrel.

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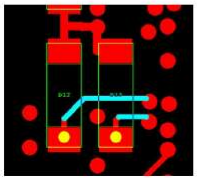
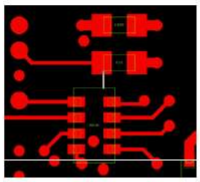
Design Issues which Affect Reliability

Assembly Examples

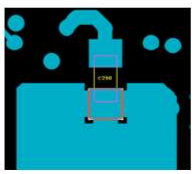
Traces under low-lying components can cause the component to rock, creating a weak solder joint. It can be sufficient to pass ICT, but no robust enough to withstand vibration.

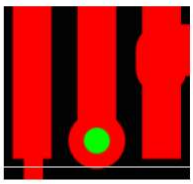




Tall components too close to adjacent components can cause shadowing at wave solder. A poor solder joint cannot easily be checked.

Different trace widths connecting pads can cause tombstoning. Partial tombstoning makes the connection susceptible to field failure.





Vias drilled through SMD pads need to be plugged. Otherwise they can have voids in the vias which can show up as intermittent opens.

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Mechanical Related Failure

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Introduction

- The solder interconnects between the package and the PCB, experience the highest susceptibility to failure under harsh loading conditions and upon failure, render the device irreversibly useless.
- The quality and reliability of solder interconnects are often considered an index of the reliability of the package on the whole.
- In addition to providing electrical connectivity, the solder joints of a BGA component also preserve the mechanical integrity of the component by serving as compliant structures between the component and the PCB.
- As a result, the solder interconnects consume a large portion of the mechanical damage caused to the assembly in a drop/shock event. Rapid shearing caused due to CTE mismatch between the component and the PCB in thermal loading scenarios and cyclic fatigue at high strain rates during shock events are attributed as major causes of failure in solder joints.

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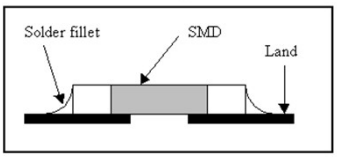
Introduction

- It has been shown that large fillets and low standoff heights of the BGA solder joints leads to an increase in their fatigue life under power cycling.



- It has been shown that large fillet angles serve to reduces high magnitudes of stress concentrations as they result in an increased in the net cross-sectional area within the joint.
- As the corner solder balls have been shown to be most vulnerable to failure in drop/shock scenarios, it has been shown that the layout of solder balls is very critical since it affects the load distribution on critical solder ball.
- The effects of solder ball metallurgy and the inter-metallic compound (IMC) thickness at the solder-copper interface and the pad surface finish has been researched, and it is shown that they affect thermal reliability performance for BGA packages.

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Reliability consideration of solder material on PCB

- Typical packaging solutions consisted in integration of Si devices onto organic packages, then assembled onto a system board using low-cost, surface-mount (SMT) compatible technologies.
- For the last two decades, solder-based ball grid array (BGA) interconnections have been the primary technology of choice for SMT assembly of microprocessor packages to printed circuit boards (PCBs).
- Package-to-board interconnections in modern consumer electronic products such as smartphones have to meet both drop and thermomechanical reliability requirements, as defined by JEDEC standards.
- The drop performance is conditioned by the ability of the solder material to absorb shock energy, driving towards **soft solders with lower elastic modulus and yield strength.**

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Reliability consideration of solder material on PCB

- The mismatch in coefficients of thermal expansion (CTE) between package and board brings cyclic strains in solder joints with variations in temperature acting as thermal loading.
- Accumulation of plastic strains under thermal cycling results in crack initiation and propagation in solder joints and, ultimately, in fatigue failures.
- Thermomechanical reliability is therefore conditioned by the ability of the solder material to prevent and accommodate plastic deformation, which is **superior in hard solders with higher elastic modulus and yield strength.**
- **Drop and thermal cycling reliabilities are consequently driving opposite material requirements for solders, but are equally critical to satisfy, bringing challenges for interconnection material design.**
- Soft solders with low Ag content such as SAC105 are found more suitable for drop testing due to their lower yield strength, modulus, and higher ductility; while hard solders with higher Ag content such as SAC305, are more favorable to thermal cycling, as illustrated below.

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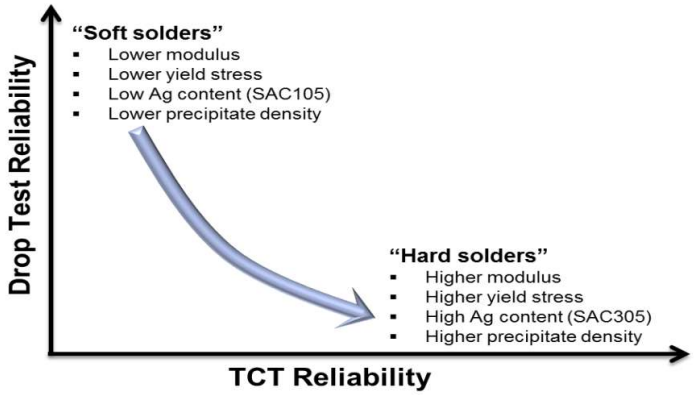
Reliability consideration of solder material on PCB



: Contrasting solder requirements for drop test and thermomechanical reliability.

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Solder Material consideration

- Among the potential candidates, SnAgCu (SAC) alloys have become prevalent over other lead-free solder systems benefitting from their low cost and superior properties such as relatively low melting point, excellent wettability, superior corrosion resistance and tailorable modulus and yield strength with variation of Ag content.
- Soft solders with low Ag content such as SAC105 are found more suitable for drop testing due to their lower yield strength, modulus, and higher ductility;
- while hard solders with higher Ag content such as SAC305, are more favorable to thermal cycling.

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Solder Materials Consideration

Advances in solder materials are, therefore, required to achieve balanced thermomechanical and drop reliability.

Solder properties are highly dependent on the alloy composition and microstructure, and can be selectively tailored by minor addition of other elements without affecting processability.

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Solder Interconnect – Pad Surface Finish

- Pad surface finishes play a critical role in determining reliable solder joint formation with excellent solderability and IMC formation.
- Some traditionally used surface finishes include hot air solder leveling (HASL), organic solderability preservative (OSP), immersion Sn (ImSn) and immersion Ag (ImAg).
- HASL, despite its excellent solderability and low cost, is non-uniform and, hence, not suitable for fine-pitch applications.
- OSP has a short operating window between assembly stages and is highly prone to oxidation.
- ImSn has concerns with tin whisker formation and ImAg requires special handling and is more expensive. Table 2.1 highlights the critical attributes and summarizes the pros and cons of the above mentioned surface finishes.

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Solder Interconnect – Pad Surface Finish

Table 2.1: Summary of pros and cons of HASL, OSP, ImSn and Imag

Surface finish attributes	HASL	OSP	ImSn	ImAg
Solderability				
Long shelf life				
Surface oxidation				
Tin whisker formation concerns				
Applicability at fine-pitch				
Uniformity/flatness				
Low cost				

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Solder Interconnect – Pad Surface Finish

- Addressing the technical limitations of above-mentioned pad finishes, two popular technologies in practice today are electroless nickel immersion gold (ENIG) and electroless nickel electroless palladium immersion gold (ENEPIG).
- With these surface finishes, two predominant intermetallics are formed, Cu_6Sn_5, and Ni_3Sn_4. Table 2.2 summarizes the primary and secondary IMCs formed with SAC solders with OSP, ENIG and ENEPIG surface finishes.

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Solder Interconnect - IMC

Table 2.2: Primary and secondary IMCs formed with common pad surface finishes

Surface Finish	Primary IMCs	Secondary IMCs
OSP	Cu_6Sn_5	Cu_3Sn
ENIG	Cu_6Sn_5, Ni_3Sn_4	$(Cu,Ni)_6Sn_5$, Cu_3Sn, Ni-Sn-P, Ni_3P
ENEPIG	Cu_6Sn_5 , Ni_3Sn_4	$(Cu,Ni)_6Sn_5$, Cu_3Sn, Ni-Sn-P, Ni_3P

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Solder Interconnect - IMC

- The thickness of the IMC formed is dependent on the reflow time and number of reflow cycles.
- According to the standards defined in JEDEC, JESD22-A104D, two additional reflows are required before initiating thermal cycling reliability testing.
- The IMCs grow further during thermal ageing or cycling.
- Presence of continuous brittle IMC layers often serves as ideal initiation sites for crack origin and propagation leading to interfacial fractures.
- IMC thickness is therefore a critical factor in determining the interfacial strength between the solder and the surface finish.
- Further, with the low % (1 – 4%) of silver in SAC alloys, brittle needle-shaped Ag_3Sn are formed in addition to Cu_6Sn_5, which are known to be detrimental to reliability performance.
- **Thus, lower IMC thickness is desired for both TCT and drop test reliability.**

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Tin Whisker – Another Mechanical Related Failure

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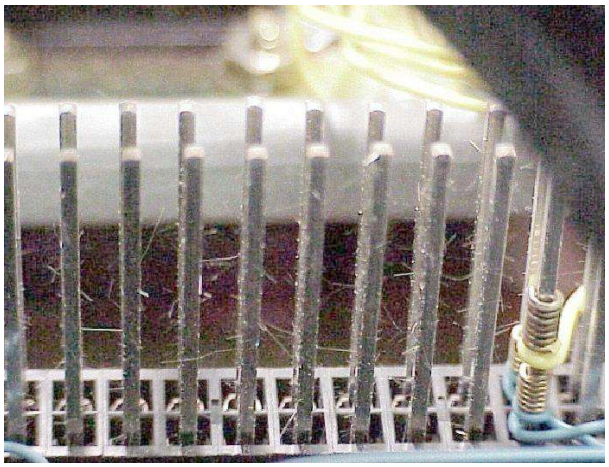
Tin Whisker Formation in Electronic Circuits



Tin-Plated Connector Pins after 10 years
Courtesy of NASA - Goddard Space Flight Center

http://nepp.nasa.gov/whisker/index.html and
http://www.klabs.org/richcontent/General_Application_Notes/tin_whiskers_ak.doc

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Problems with Whisker

- Tin whisker can carry up to 25 mA and can sustain a few tenth of V/mm before burning out.
- This short circuit are of intermittent type and will cause failure in today low voltage electronic equipment.
- For high current circuit, the whisker are quickly burnt out and may not pose as serious a threat as in low power circuits.

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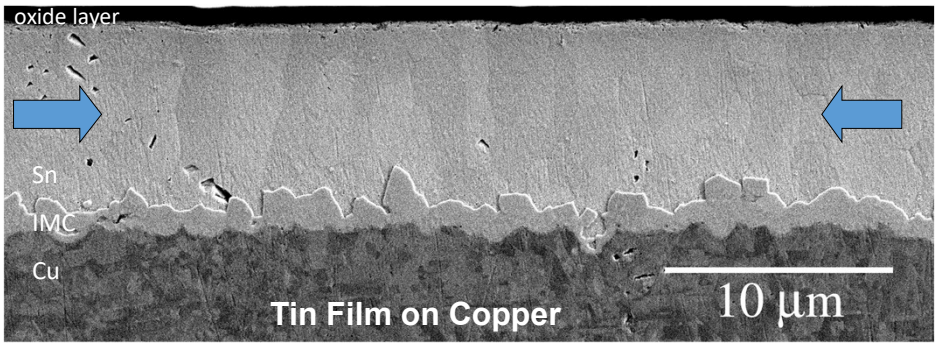

- Compressive stress in electrodeposited Sn film
- Intermetallic compound (IMC) growth of Sn on Cu believed to increase compressive stress in Sn film
- Stress relief mechanisms depending on film composition, creep, grain structure, IMC, …
- Local fracture of oxide film, corrosion, … implicated in nucleation

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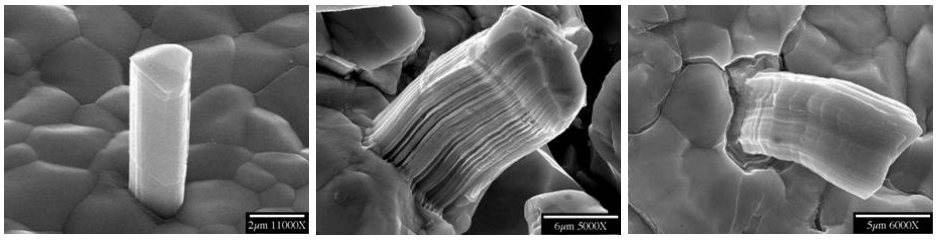
Manifestations of Stress Relaxation



Filament with consistent cross-section (columnar)

Striations

Rings

From iNEMI Modeling Group

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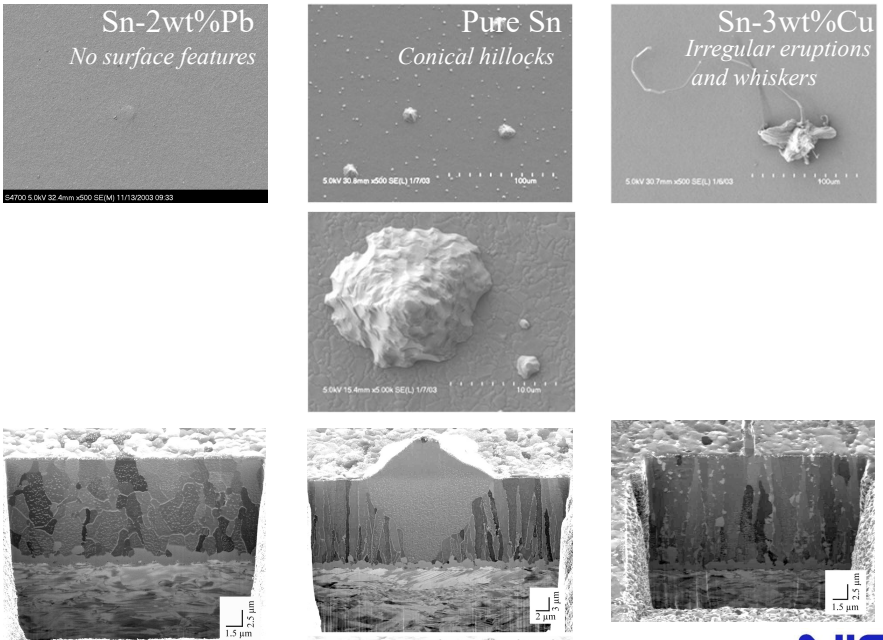
Microstructure of Surface & Interior of 16 µm Thick Deposits @ >100 days



FIB pictures: Galyon and Palmer

NIST

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Thermal Related Failures

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Thermal Performance

- Electronic Package dissipates heat along two paths: (1) convection and radiation off the exposed surface of the package and (2) conduction into and through the PCB followed by convection and radiation off the exposed board surfaces.
- Of the two heat dissipating paths, the most significant is through solder joints to the PCB board.
- Because of this, thermal performance is determined by the number of solder joints, joint size, pitch, PCB construction, and density of on-board copper traces, as well as presence of thermal vias connecting solder joints to the PCB ground plane.

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Thermal Aging

- Drop induced interconnect failure is a major reliability concern for portable electronic applications
- Impact reliability is function of material characteristics and system level component layout
  - Layout and support for the PCB cause non-uniform stresses under impact
  - The impact loading leads to brittle intermetallic fracture at package to solder joint interface
- Cumulative failure data fit well to Weibull distribution

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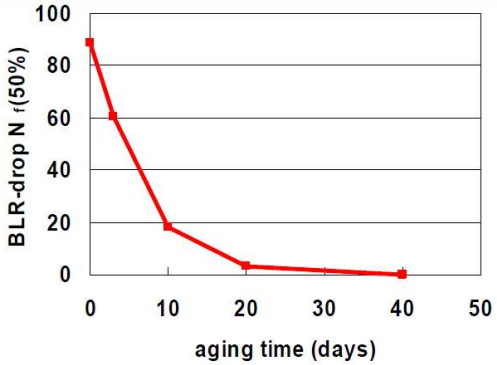
Thermal Aging



- Drop reliability degrades significantly after 125°C/10 days aging
- BLR-drop dependency on component location is not observed for the case of 40 days aging
  - All components failed within 2nd drop after 40 days aging

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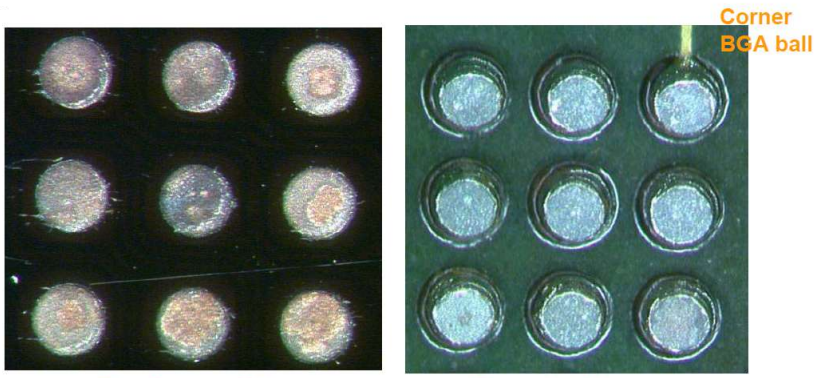
Thermal Aging

Drop failure fractograph (125°C/40-days)



Multiple joints showing package/solder IMC fracture

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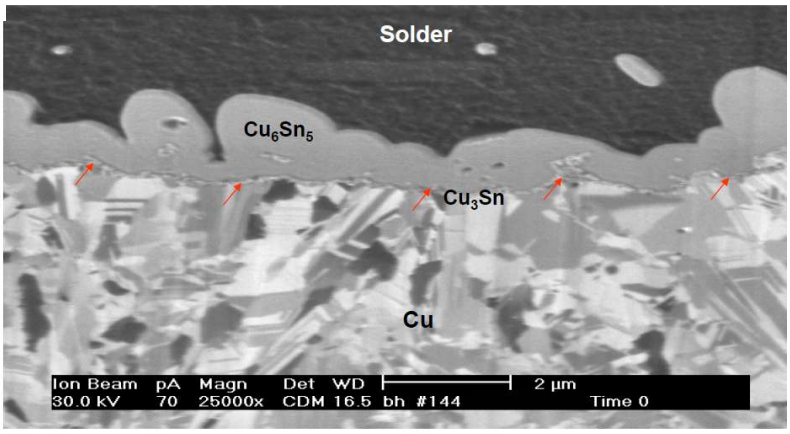
Thermal Aging

Cu/SnAgCu interface (time zero)



- Cu_6Sn_5 scallops were observed at the pad/solder interface.
- A thin layer of Cu_3Sn also formed
  - required by thermodynamic equilibrium.

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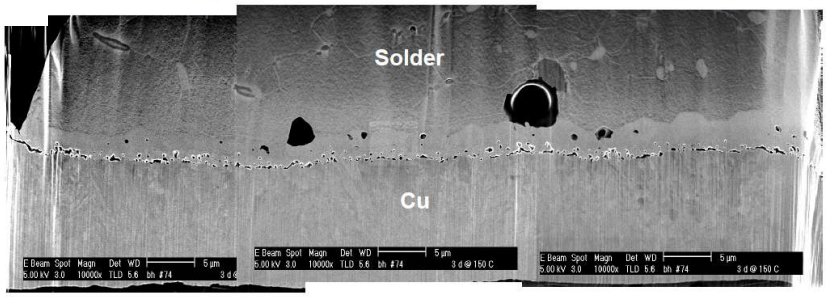
Thermal Aging

Cu/SnAgCu interface (150°C/3 days)



- During solid state aging, inter-diffusion of Sn and Cu occurred
  - Cu being the dominant species.
- After only 150°C/3days baking, Kirkendall voids at Cu/Cu_3Sn interfacial region grew to large disk-like cracks.
  - The largest void was around 4µm.

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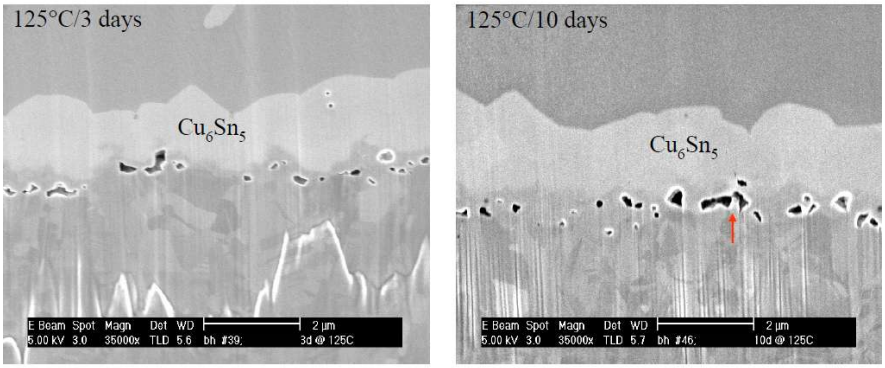
Thermal Aging

Cu/SnAgCu interface (125°C/3 & 10 days)



After 125°C/10 days, the largest voids were about 1 μm, indicated by the red arrow.

47

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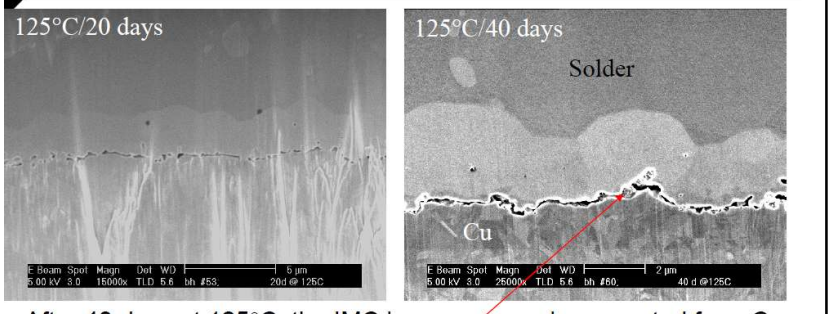
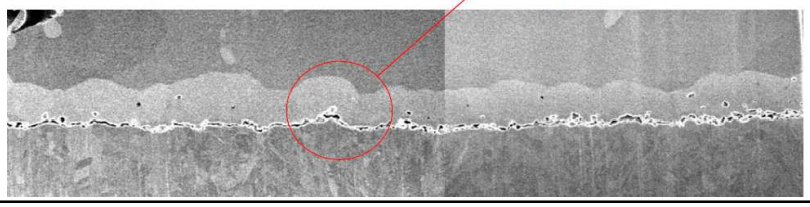
Thermal Aging

Cu/SnAgCu interface (125°C/20 & 40 days)



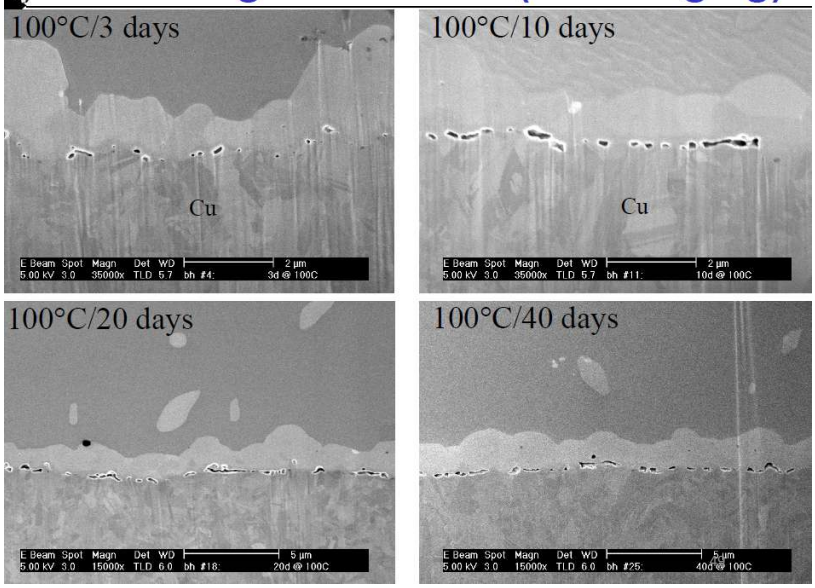
After 40 days at 125°C, the IMC layer was nearly separated from Cu



48

Thermal Aging

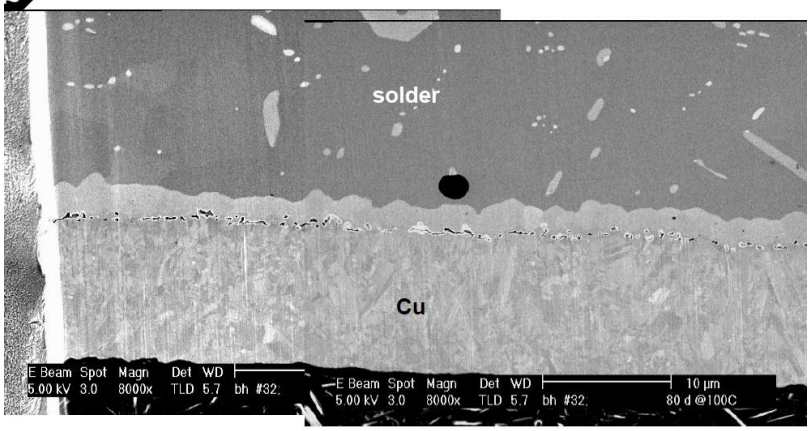
Cu/SnAgCu interface (100°C aging)



49

Thermal Aging

Cu/SnAgCu interface (100°C/80 days)



Voiding at 100°C/80 days was better than after 125°C/40 days, but similar to 150°C/3 days. 50

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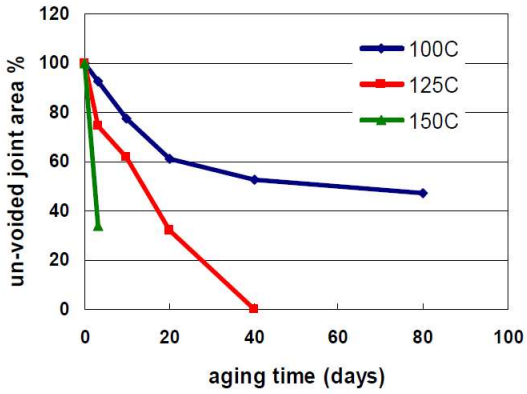
Thermal Aging

Remaining interfacial IMC ligaments after aging



Voiding density and size were collected from cross-sectional analysis, and then converted to estimate the density in joint area

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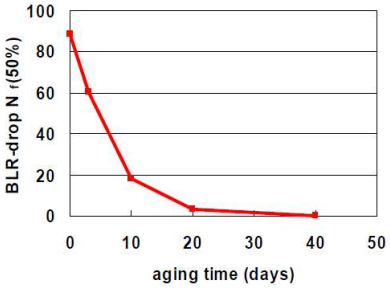
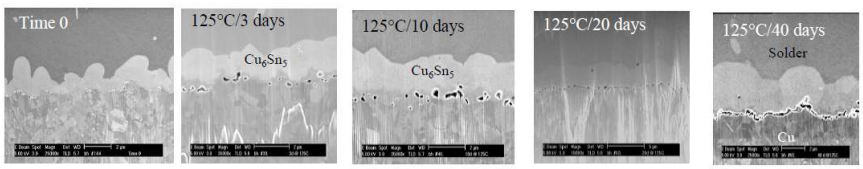
Thermal Aging

Correlation of drop reliability to IMC voids





Strong correlation is observed between interfacial voiding and drop reliability degradation

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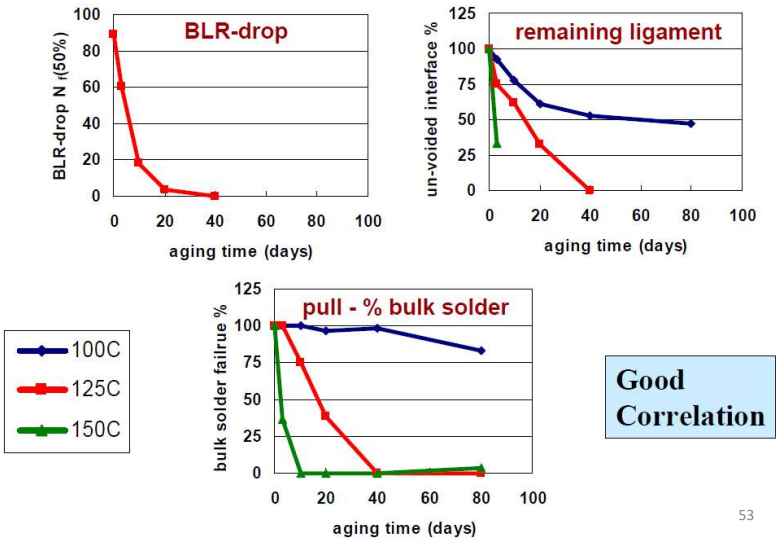
Thermal Aging

Correlations between voids, pull, shear and drop tests



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Summary

Very strong correlation between drop reliability and voiding for Cu/SnAgCu solder interface

- Kirkendall voids at Cu/Cu_3Sn interface are detrimental to the drop reliability after aging
  - Similar trend is expected for temperature cycling reliability
- Voiding process is activated at as low as 100°C
- Bare Cu or OSP-Cu surface finish is not suitable for higher temperature applications

- Ball shear testing does not correlate to drop test performance. Ball pull strength is not a good indicator of shock reliability either
  - The only parameter correlating to BLR-drop was the percentage of bulk solder failure in ball pull testing
  - Alternative component level testing technique is needed
    - ex. laser spallation, water jet impact, etc

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Solder Migration

- *Solder migration may occur during flip chip processing, reliability* testing or operational life.
- Solder migration during processing is generally caused by voids, or delamination next to a joint, and is more common in processes where the cure step is done at high temperatures or after thermal excursions.
- These cure steps are common to some underfill materials that require long high-temperature cures or materials that cure during a reflow cycle, such as snap-cure underfills and no flow underfills.
- Solder migration also occurs in parts exposed to multiple reflows during processing or preconditioning.
- Migration can also occur in reliability testing when the solder joints are given time to creep, especially in air-to-air thermal cycling.
- In all cases, solder migration is due to the expansion of the solder at high temperatures, combined with a void adjacent to the solder.
- As the solder expands, or conversely the underfill shrinks, the solder is forced into the void. The solder relieves internal pressure by extruding into the adjacent void.

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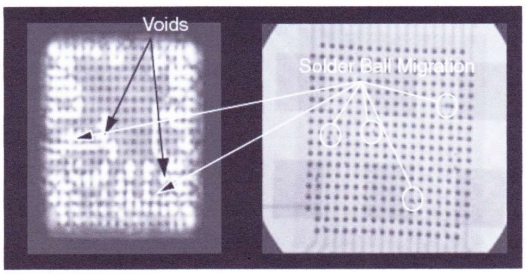
Solder Migration

FIGURE 9.26 Solder ball migration due to voids caused by the cure. C-SAM image on left and x-ray on the right.



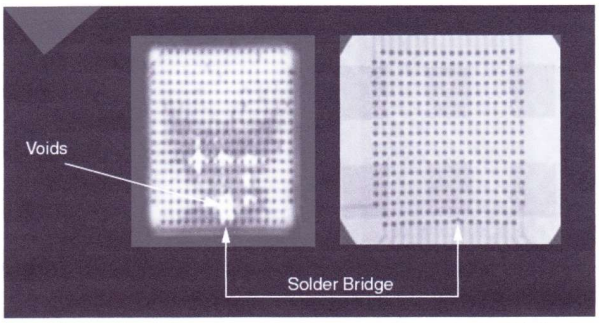


FIGURE 9.27 Solder bridge in a capture void that occurred during underfill dispensing. C-SAM (left) and x-ray (right).

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Thermo-mechanical Related Failures

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Temperature Excursion of Electronics

Table 1-1 Thermal environments for electronic products

Use condition	Thermal excursion (°C)
Consumer electronics	0 to 60
Telecommunications	-40 to 85
Commercial aircraft	-55 to 95
Military aircraft	-55 to 125
Space	-40 to 85
Automotive-passenger	-55 to 65
Automotive-under the hood	-55 to 160

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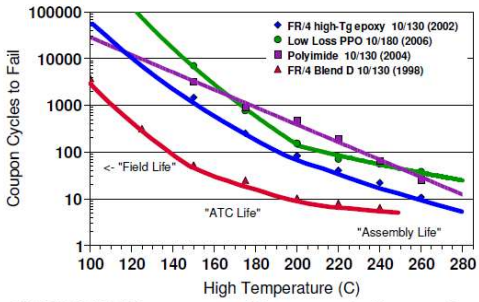
Reliability of Plate-through hole

- The CTE mismatch between copper barrel and the surrounding laminate at reflow temperatures can produce deformation of such magnitude that even well plated vias can survive only a handful of assembly passes without cracking.



Select CITC PTH life curves to illustrate challenge of unfilled wiring vias.

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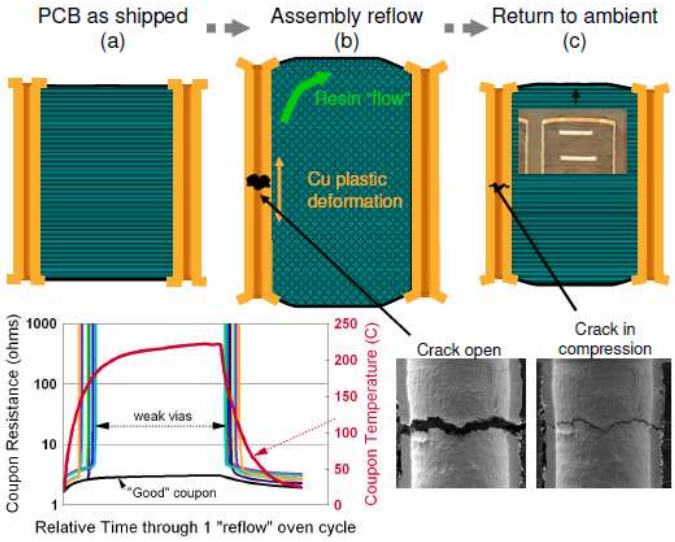
Reliability of Plate-through hole



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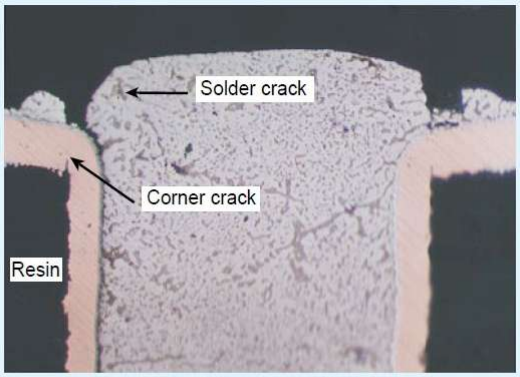
Differences With and Without Solder



Test conditions: Temperature Cycle Test
–65°C ↔ +125°C, 30 min. each, 500 cycles

Photo. 1 Cross section observation results (with solder) (200×)

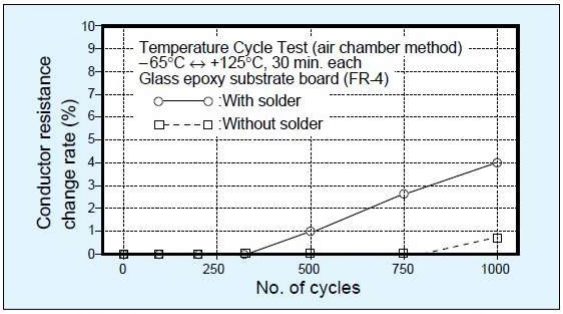


Fig. 3 Changes in conductor resistance with and without solder

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Differences Due to Temperature Conditions

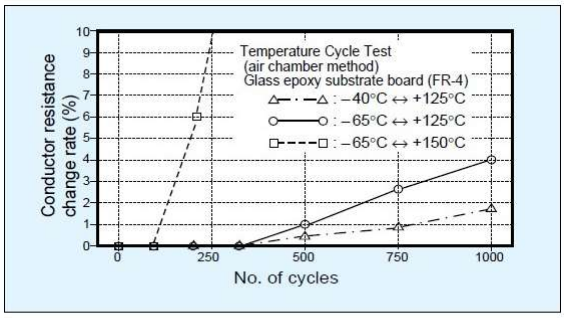
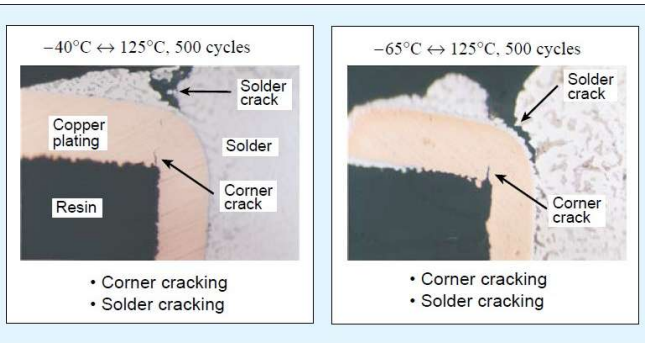


Fig. 4 Changes in conductor resistance for each temperature



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Differences Due to Temperature Change Time

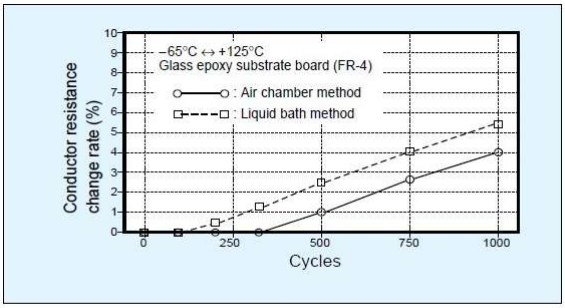

Fig. 5 Changes in conductor resistance due to air chamber method and liquid bath method

Observing the cross sections indicates that the failure mode is corner cracking in both tests, but deformation of the copper plated section occurs in the Thermal Shock Test, leading us to assume strong stress. (Photo. 3)

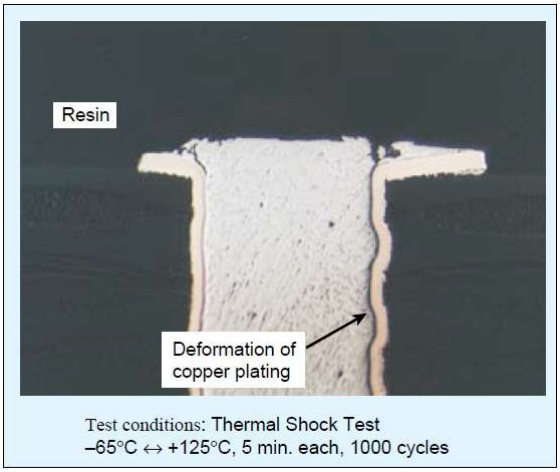

Photo. 3 Results of cross section observation (100×)

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However, due to high temperature and stress the solder also sustains roughening of the intergranular boundary, loses shear force and tractive force, and finally ruptures. Then, the stress is concentrated in the corner, promoting cracking and leading to a complete break. Photo. 4 shows this process.

Photo. 4 Corner cracking process (500×)

Corner cracking is strongly related to solder cracking, and so through hole reliability can be improved by suppressing cracking.

The greater the test temperature difference, and the faster the temperature change time, the faster the through hole degradation.

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Thermal induced delamination

- Thermally induced internal delamination is one of the original and ever-present failure mechanisms for laminate substrates and boards.
- The root cause is generally linked to the "explosive" vaporization of entrapped moisture at high temperatures, especially reflow.
- The alternate names of blistering or popcorning not only reflect the mechanism but also hint at another fortunate attribute— when they occur within laminates of any thickness they create a measureable opening within the substrate that is almost always visible at the surface as a raised and/or discolored area.
- "Visible delamination" as such is typically observed in open areas with few vias, and/or in regions surrounding vias

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Thermal induced crack – Eyebrow Crack

- All three mechanisms are dependent in some way on choice of laminate material, reflow peak temperature, PWB processing, and total cycles, but otherwise they are significantly different in key ways, which affects how and where they need to be considered in design and evaluation.

Table 3-- Comparison of today's laminate failure mechanisms

Attribute	Visible delamination	Invisible delamination	Eyebrow cracks
Geometry vs. temperature	Open at peak as formed, open at ambient	Closed at peak as formed, open at ambient	Open at peak as formed, closed at ambient
Locations where mechanism is active	Open areas (no vias) or loose grids	Dense, tight grids of thru vias	Above, below, or between buried vias.
State of stress during formation	Neutral	Compressive	Tensile
Aspect ratio and/or thickness dependence	None	Yes, both.	Yes, likely function of via dia & length.
Moisture/bake influence	Yes, to a point	Yes, to a point	No
Non-destructive inspection/screen	Yes, almost always.	No	No
Typical interface fractured	Resin to glass	Resin to resin	Resin to resin

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Delamination

- Figure 5.12 shows two edge delaminations between the underfill and the die, and between the underfill and the substrate, in a flipchip assembly of ICs.

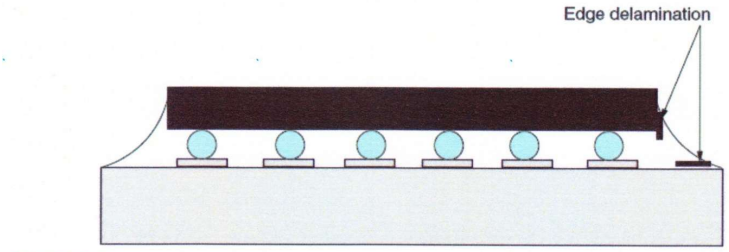

FIGURE 5.12 Edge delaminations in a flip-chip assembly with underfill.

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Thermo-mechanical Failure Mechanisms

- Electronic packages are complicated material systems operating under electrical, thermal and mechanical loading conditions.
- Many of these materials are organic materials that have highly nonlinear properties, and that are very process and scale sensitive.
- These complex mechanical systems usually lead to complicated failure mechanisms.
- Figure 22.6 demonstrates many failure modes of a FC PBGA (flip chip plastic ball grid array) package. Other failure modes exist but are not listed.

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Thermo-mechanical Failure Mechanisms

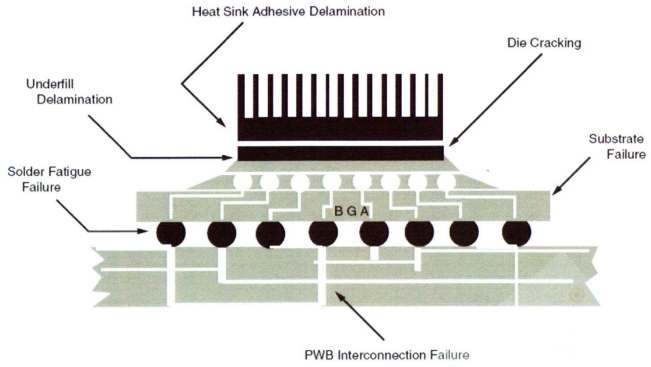

FIGURE 22.6 Typical failure modes in a FC PBGA package.

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Thermo-mechanical Failure Mechanisms

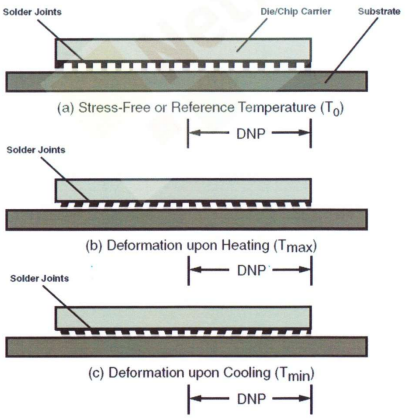

FIGURE 5.3 An illustration of thermomechanical deformation in solder joints. (a) Stress-free or reference temperature (T_0), (b) deformation upon heating (T_{max}), (c) deformation upon cooling (T_{min}).

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Electrical Related Failures

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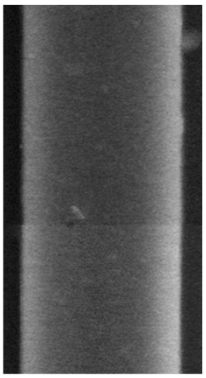
Electromigration



Cher Ming Tan, “Electromigration in ULSI Interconnections”, World Scientific Publishing, 2010

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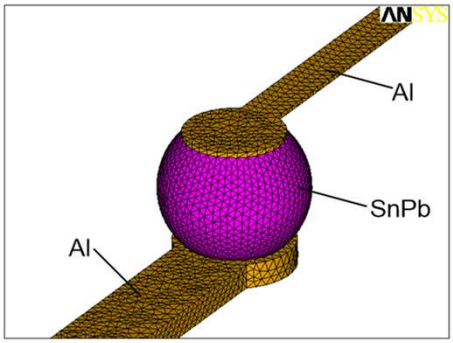
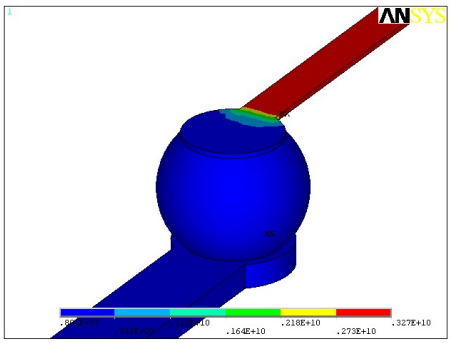
Solder Bump Electrical-Thermal-Mechanical Simulations



FEM model



Current Density Distribution (pA/μm^2)
Total Current in Solder Bump=650mA

Bump Diameter: 100μm
Upper Al Stripe Width:40μm, thickness:2μm
Lower Al Stripe Width:80μm, thickness:25μm

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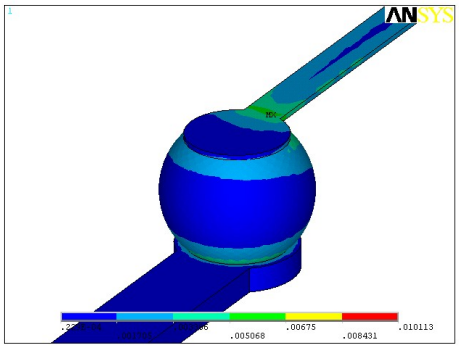
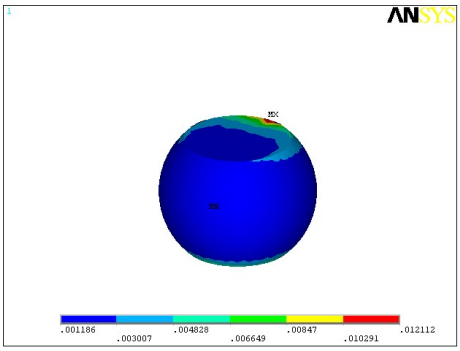
Thermal gradient (K/μm)



With Al stripes



With Al stripes removed

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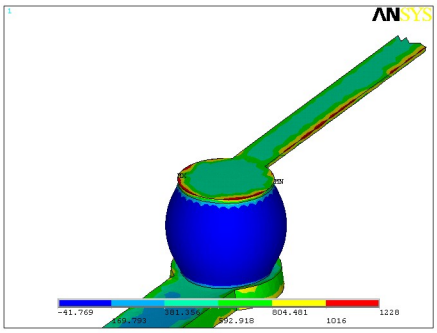
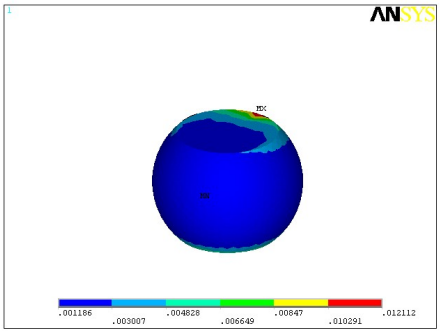
Thermo-mechanical Stress & Gradient



Thermo-mechanical stress (MPa)



Thermo-mechanical stress gradient (MPa/μm)

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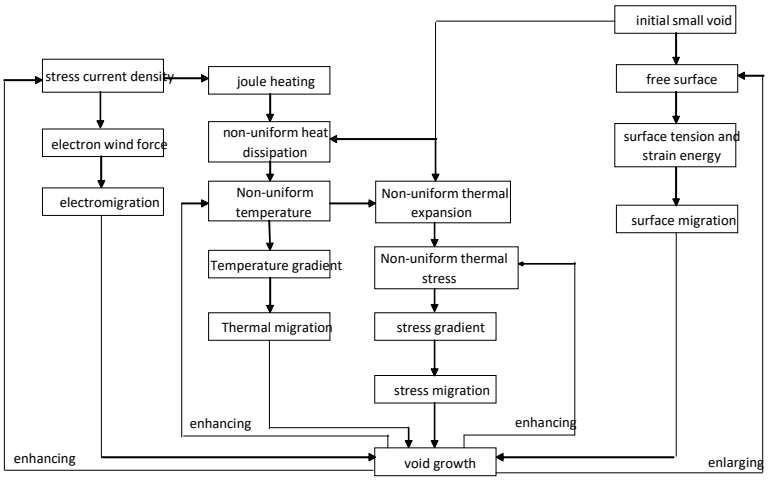
Numerical modeling of EM



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Humidity Related Failure

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Moisture and boards

- The effects of moisture are not limited to the popcorning of active components; equivalent effects may be found with PCBs exposed to moisture and then soldered.
- Where damp boards are not thoroughly dried beforehand, they may delaminate during soldering, or at the very least there will be problems, such as solder balling on reflow and spitting and solder voids on wave soldering.
- As with popcorning, most of the moisture-related issues are exposed during assembly.
- However, moisture can have an ongoing impact on circuit performance by affecting the electrical characteristics of the laminate. The higher the ambient relative humidity, the greater the moisture on the surface as well as in the bulk of the material.
- It is reported that the surface resistance expressed in ohms/square can vary as much as 4–5 orders of magnitude over a 30-90% relative humidity range. Dielectric losses also increase with increasing moisture content.

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Moisture and boards

- From this, one might suppose it better to keep parts dry, and assemble in a dry atmosphere. However, at humidities below 30%, static charging problems become severe.
- As a compromise, most fabrication and assembly shops operate at a relative humidity of around 50%.
- The common failure mechanisms attributed to moisture absorption in PCB are:
  - Entrapped moisture can cause blistering or inner layer delamination
  - Excessive moisture increases dielectric constant and dissipation factor leading to changes in circuit switching speed.
  - Since moisture acts as a plasticizer, it reduces the glass-transition temperature (Tg), which in turn increases stresses on PCB features such as plated through-holes
  - Oxidation of copper surfaces leading to poor wettability of finishes and solder
  - **Ionic corrosion causes electrical opens or shorts**
  - **Interfacial degradation can result in a reduced time to failure due to conductive filament formation (CFF)**

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Chemical and Electrochemical Failures in PCB

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Corrosion

- If there is sufficient moisture, that is several monolayers of moisture, a local corrosion cell is set up with oxidation at the anode and reduction at the cathode occurring.
- The oxidized metal ion in the presence of a suitable anion forms an oxide or corresponding salt. This is called the corrosion product.
- This process continues and the corrosion product builds up toward the opposite conductor.
- The corrosion product could either be soluble in the conducting medium or an insoluble product depending on its chemical composition.

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Corrosion

Table 6.5 Standard Oxidation Electrode Potentials for Metals of Importance in Electronic Packaging

Metal	Metal Ion in Equilibrium	Electrode Potential at 25°C/V
Gold (Au)	Au^{3+}	1.498
Platinum (Pt)	Pt^{2+}	1.2
Palladium (Pd)	Pd^{2+}	0.987
Silver (Ag)	Ag^{+}	0.799
Copper (Cu)	Cu^{2+}	0.337
	Cu^{+}	0.521
Lead (Pb)	Pb^{2+}	−0.126
Tin (Sn)	Sn^{2+}	−0.136
Nickel (Ni)	Ni^{2+}	−0.250
Iron (Fe)	Fe^{2+}	−0.440
	Fe^{3+}	0.331
Indium (In)	In^{3+}	−0.342
Chromium (Cr)	Cr^{3+}	−0.744
Aluminum (Al)	Al^{3+}	−1.662
Magnesium (Mg)	Mg^{2+}	−2.363
Gallium (Ga)	Ga^{3+}	−0.53

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Electrochemical Corrosion

- A different phenomenon is generally observed under the influence of applied DC bias voltage.
- The anode-cathode designation is, however, decided by the polarity of the applied DC potential. In this case also, as in the case of corrosion, oxidation of the metal occurs at the anode.
- The positively charged ion, under the influence of the applied potential travels through the conductive medium between the conductor interspace toward the negative electrode.

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Electrochemical Corrosion

- At the negative electrode the positively charged ion is reduced to a neutral metal atom. This reduction process at the cathode or negative electrode continues. This growth of metal at the cathode appears as filamentary dendrites with a characteristic needle-like appearance.
- The growth continues until the anode is depleted or the dendrite reaches the anode which results in an electrical short.
- It is to be noted that three conditions must be met for metal migration to occur: sufficient moisture, presence of an ionic species for a conductive path, and an applied potential. The dendrite growth occurs along well-defined crystallographic axes that are characteristic of the element in question.

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Electrochemical Migration on PCB

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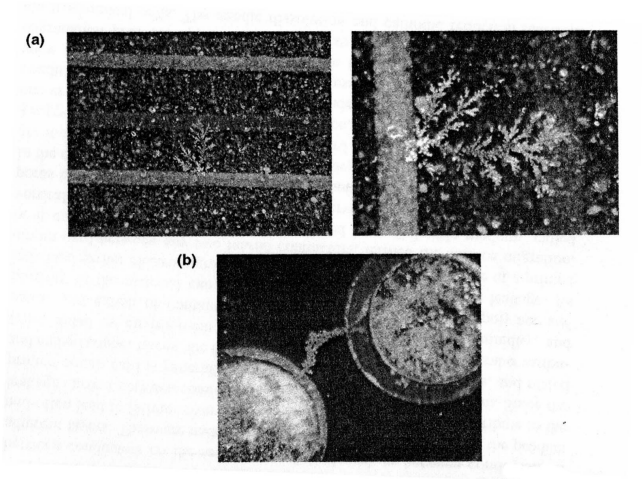
Electrochemical migration - Dendrite



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Electrochemical migration - Dendrite

- As the electronic package assemblies utilize finer and finer pitch components, spacing between conductors become smaller and smaller, and the voltage gradients between conductors become steeper compared to coarse pitch component assemblies.
- In the presence of steeper voltage gradients ionic species migrate faster to their respective electrodes, hastening failure times to cause potential failure.

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Increasing risk of ECM

- ANSI / ASRAE water standards finds that 3 monolayers of adsorbed water will mobilize an ion.
- They also report environmental conditions require roughly 50-60% RH (relative humidity) to obtain 3 monolayers of moisture.
- As circuits continue to miniaturize, the distance between conductors narrows. This has relevance in that shorter distances results in lower levels of ions needed to be mobilized in 3 monolayers of water to create a reliability issue. As such, residues residing under Bottom Terminated Components (QFN and LGA style components) increase reliability risks.

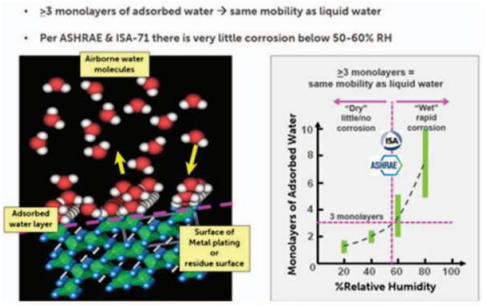

Figure 5: ANSI / ASHRAE Monolayers as a function of RH[5]

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Acceleration factor of Ionic Migration

Factor	Acceleration condition
Materials	Fast Ag Cu Pb Sn-Pb Solder Sn Au Slow
Temperature	High Temp
Humidity	High humidity
Voltage	High voltage
pH	Acidity
Ionic impurities	Halogen material (Chlorine, Bromine)
Printed-cuircuit board material	Paper phenol > Glass epoxy > Polyimide > Ceramic

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Electrochemical Failure Modes

- Conductive Anodic Filament Growth.
  - Conductive anodic filament growth (CAF) causes electrical shorts when a metal that dissolves anodically is redeposited at the interface between the glass (or other) fibers and the resin matrix of a printed circuit board.
  - Conductive anodic filament growth is promoted by delamination at the glass-polymer interface, which may in turn be promoted by various environmental stresses including high temperatures (greater than about 260°C for FR-4) and thermal cycling.
  - Shorts seem to occur most rapidly within a single fiber bundle connects two pads.

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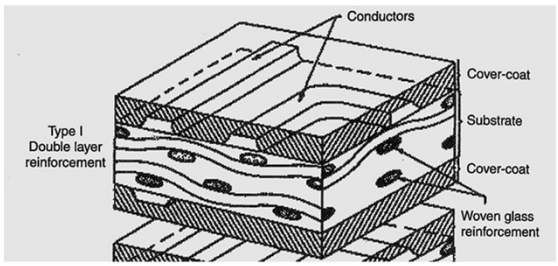
Electrochemical Failure Modes



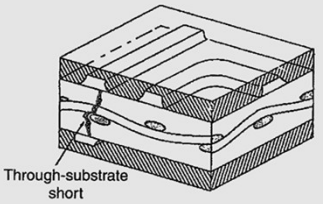


FIGURE 56.2 Through-substrate short.[2] © 1976 IEEE

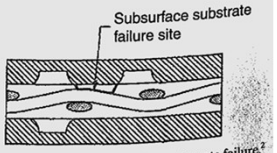


FIGURE 56.3 Subsurface substrate failure.[2] © 1976 IEEE

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Electrochemical Failure Modes

- Factors that affect CAF formation:
  - Substrate material (in the order of susceptibility)

    MC-2 > Epoxy/Kevlar > FR-4 ~ PI > G-10 > CEM-3 > CE > BT

    (PI – polyimide/woven glass; G-10-non-fire-retardant epoxy/woven glass; CE-cyanate esters; BT-bismaleimide triazine)
  - Processing such as drilling, depaneling, soldering etc.
  - Voltage and spacing
  - Soldering flux
    - Polyglycols (found in water-soluble fluxes) diffuse into the epoxy during soldering increases the moisture uptake.
  - Humidity threshold below which no CAF depends on operating voltage and temperature.

Test method: IPC-TM-2.6.25

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Recent case study

Figure 1. Visual appearance of the failed PCB from field returns.

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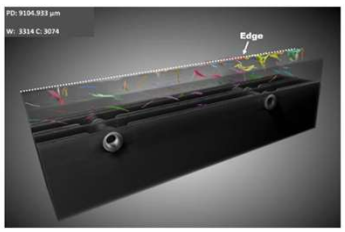
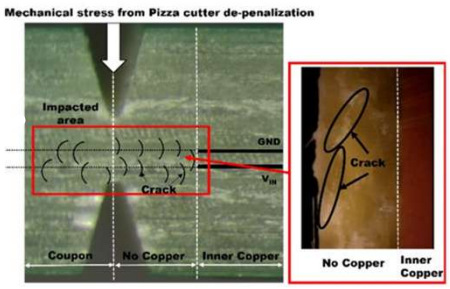
Cracks generation due to de-paneling



Micro-CT identification of 78 individual microcracks near the V-cut boundary



Localized crack formation along the board edge after de-panelization

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Verification of Solution

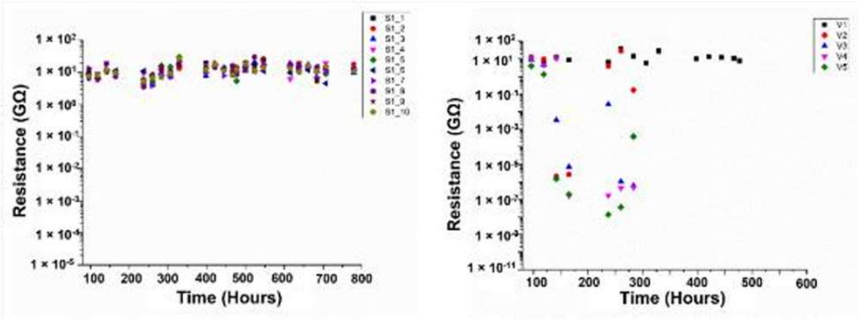

Figure 11. THB reliability test results comparing V-cut and improved de-panelization methods.

Tan, C.-M.; Chen, H.-H.; Wu, J.-P.; Sangwan, V.; Tsai, K.-Y.; Huang, W.-C. Root Cause Analysis of a Printed Circuit Board (PCB) Failure in a Public Transport Communication System. Appl. Sci. 2022, 12, 640. https://doi.org/10.3390/app12020640

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Thank you for your attention

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