LOW POWER DIGITAL EQUALIZATION FOR HIGH SPEED SERDES

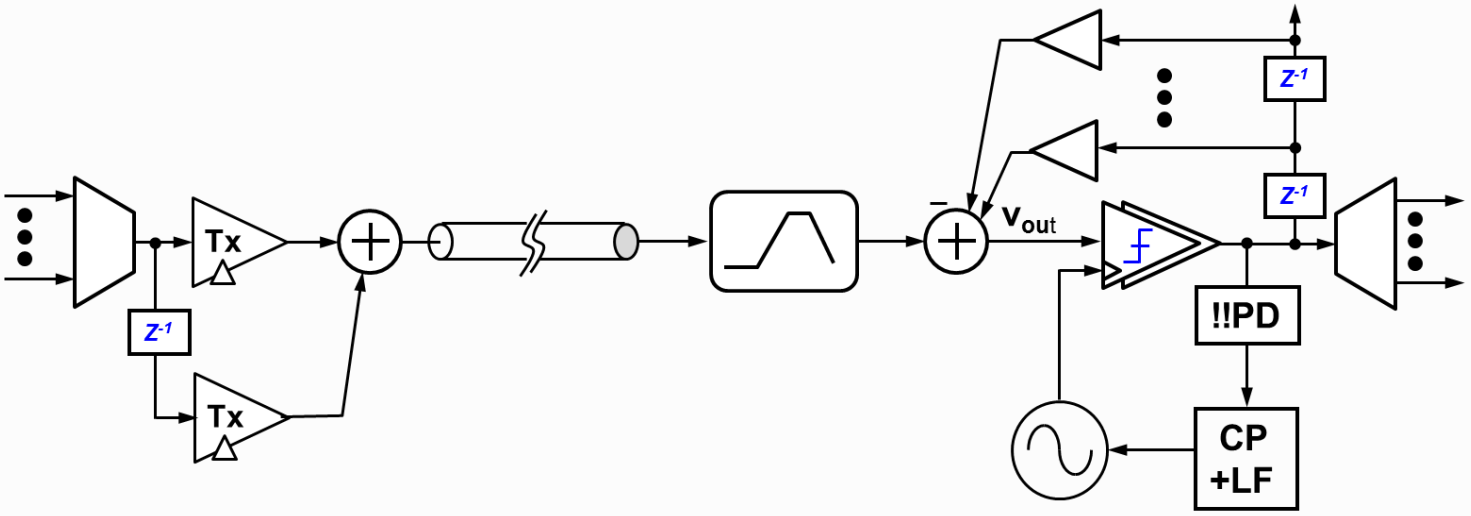
Masum Hossain

University of Alberta

Outline

- Why ADC-Based receiver?
- Challenges in ADC-based receiver
- ADC-DSP based Receiver
  - Reducing impact of Quantization Noise
  - Variable Resolution ADC
  - low-latency high-resolution TDC-based timing recovery
  - Implemented Prototype and Measured Results

Conventional mixed-signal Link



Tx FIR Filter:
- Peak power constrained
- Limited by supply voltage

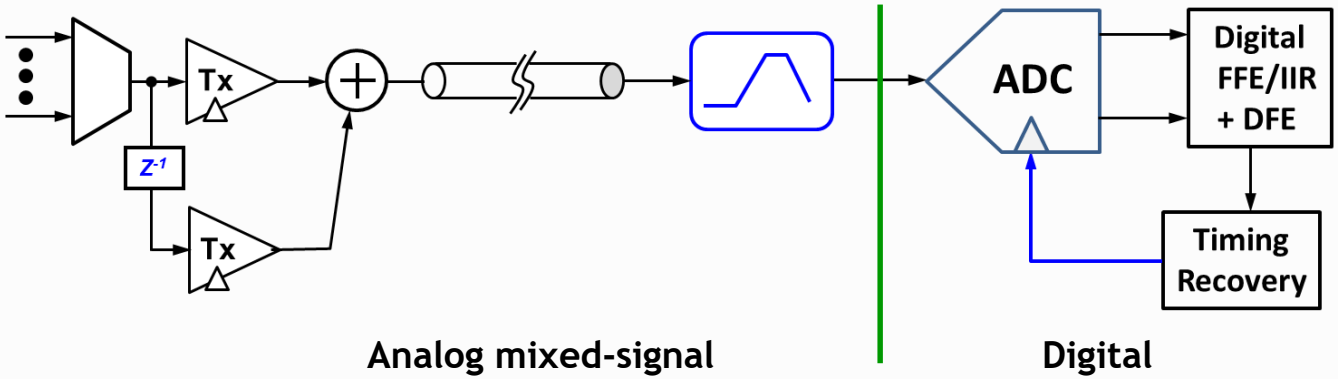
Peaking equalizer:
- Analog - does not scale well
- Limited by supply voltage
- PVT variation

Decision Feedback Eq.:
- Latency constrained
- Difficult for multilevel signaling

Existing equalization strategy does not scale well with technology, channel loss and data rate

Mixed-signal vs ADC-based Link

ADC-based high speed Link



Benefits of DSP-based equalization:

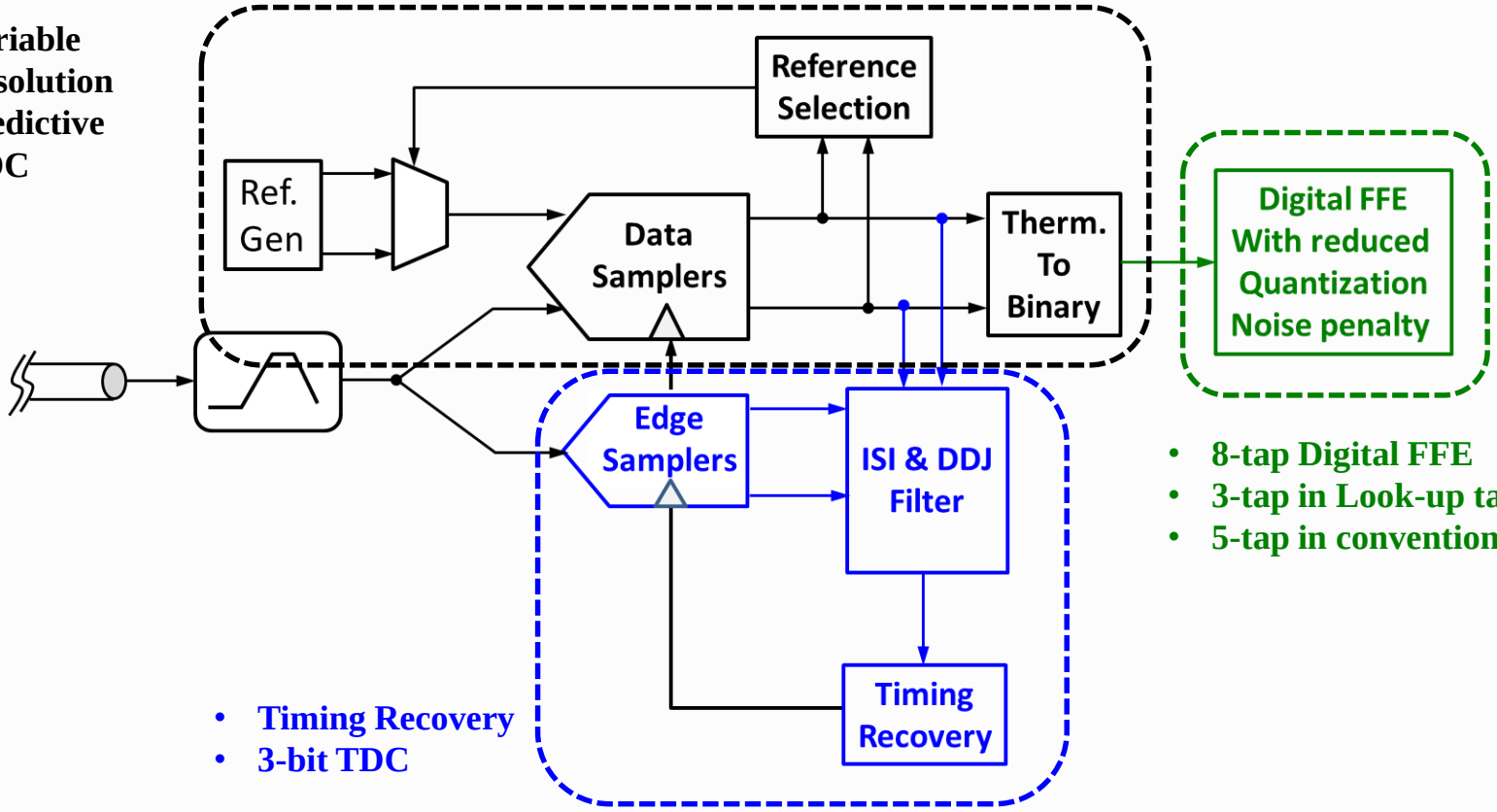
- Scales well with technology
- Frequency response can be well controlled
- Can equalize both pre and post cursors

Challenges of DSP-based equalization:

- ADC-DSP is power hungry.
- Higher loop latency make timing recovery difficult

PAM-4 Digital Receiver Architecture

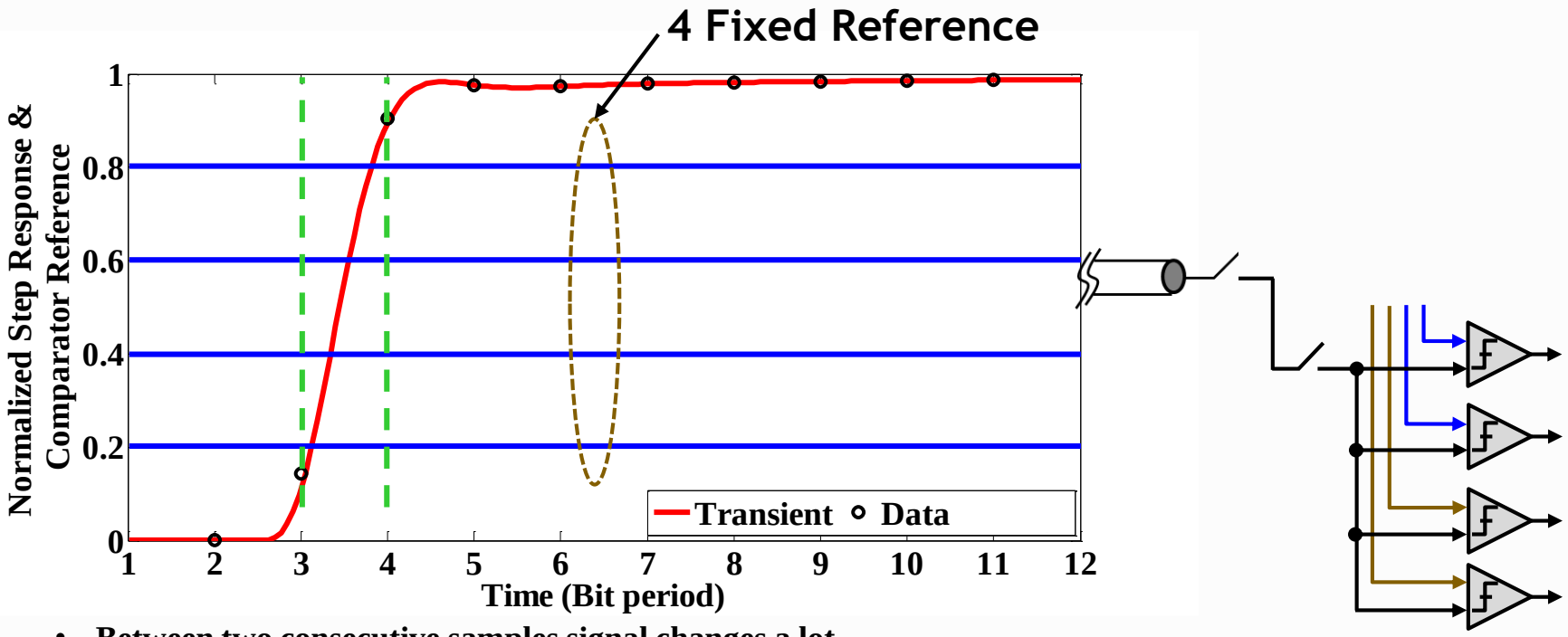
- **Variable Resolution**
- **Predictive ADC**



- **8-tap Digital FFE**
- **3-tap in Look-up table**
- **5-tap in conventional way**

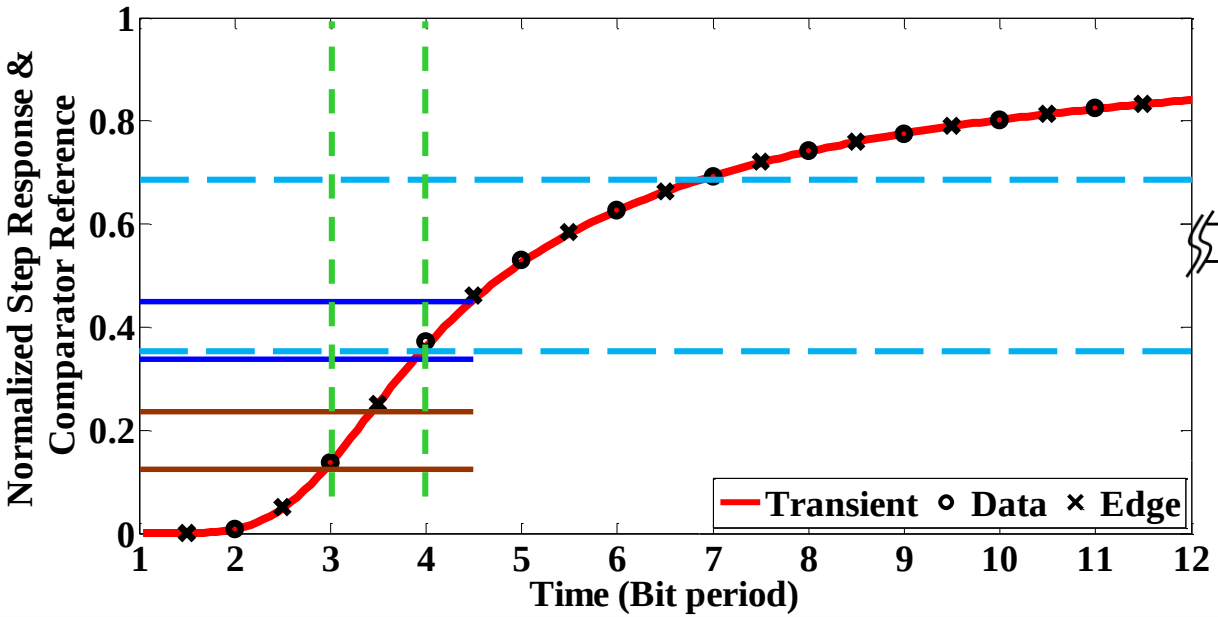
- **Timing Recovery**
- **3-bit TDC**

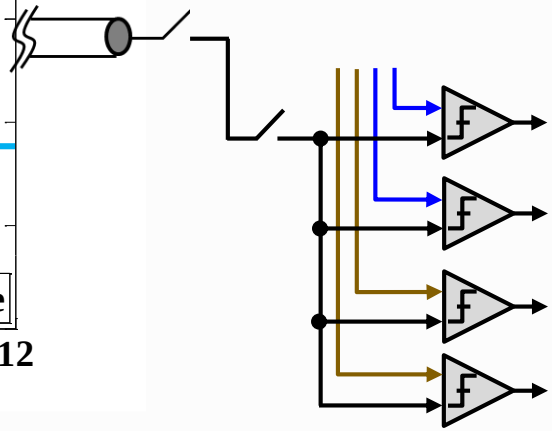
Variable Resolution ADC - 12 dB loss



- Between two consecutive samples signal changes a lot
- Need to cover entire dynamic range - **4 Fixed References.**

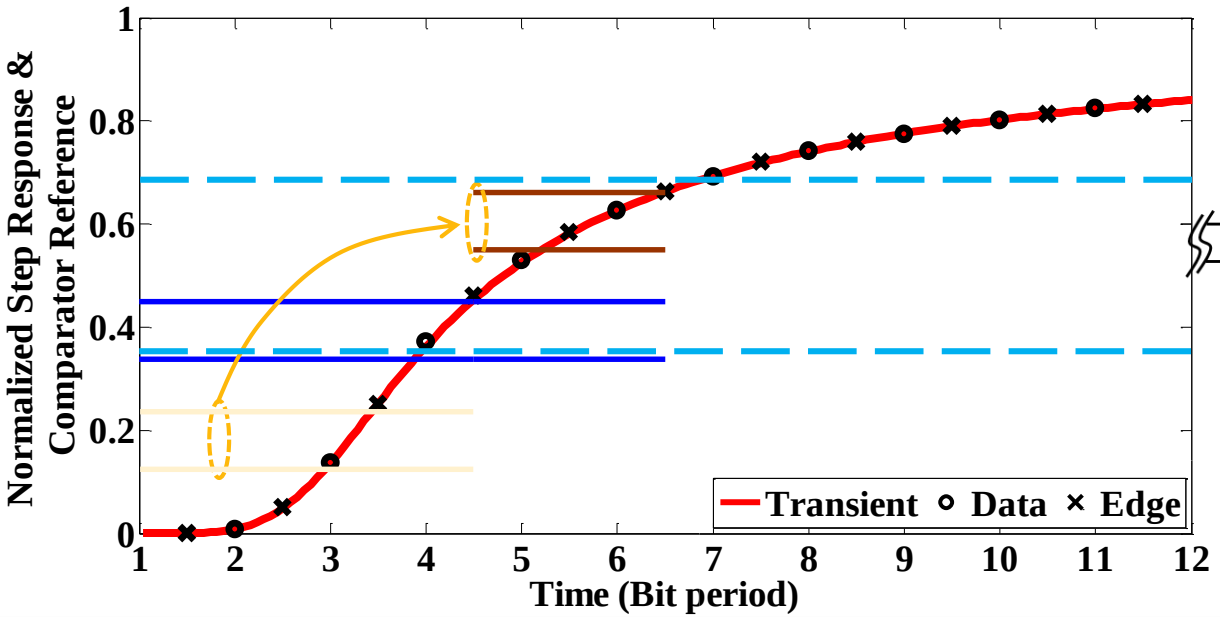
Variable Resolution ADC - 25 dB loss

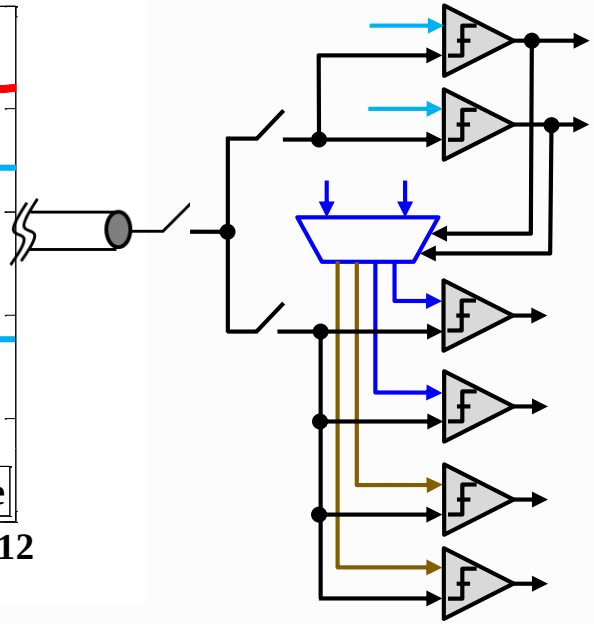




- Between two consecutive samples signal changes around 20% - 30%
- Need to cover a portion of entire dynamic range – Reference Switching

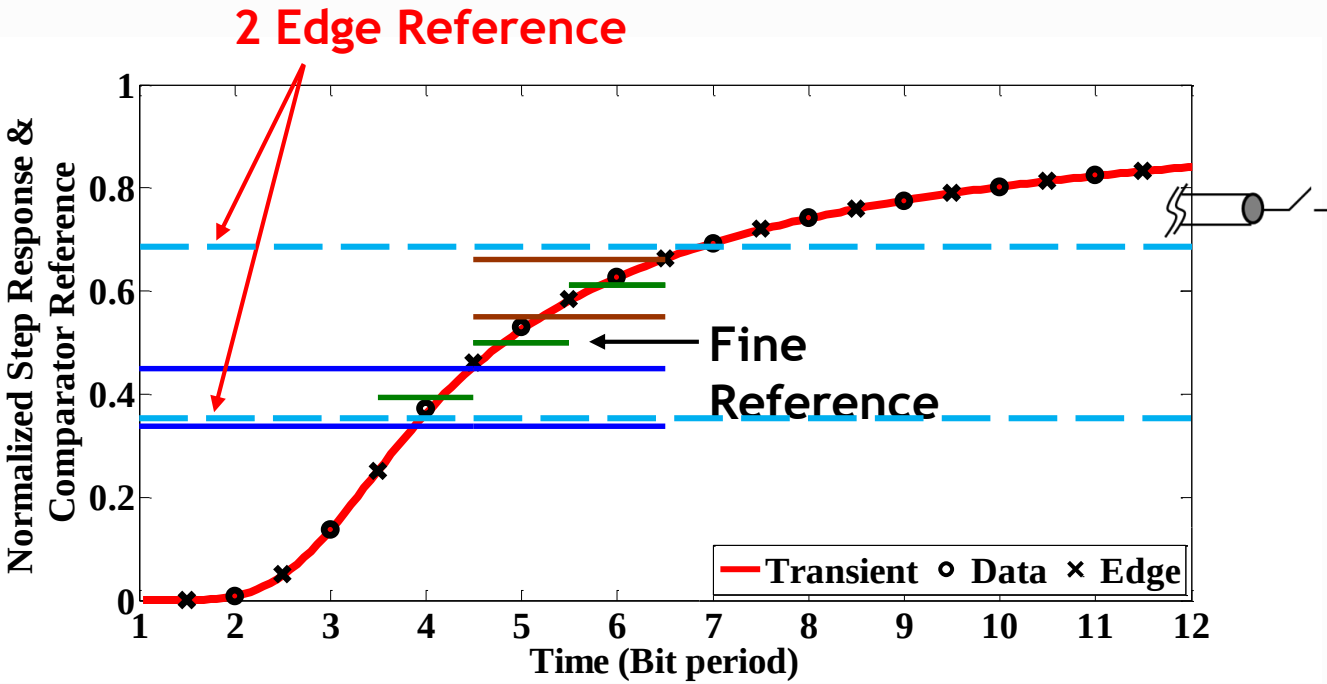
Variable Resolution ADC – 25 dB loss

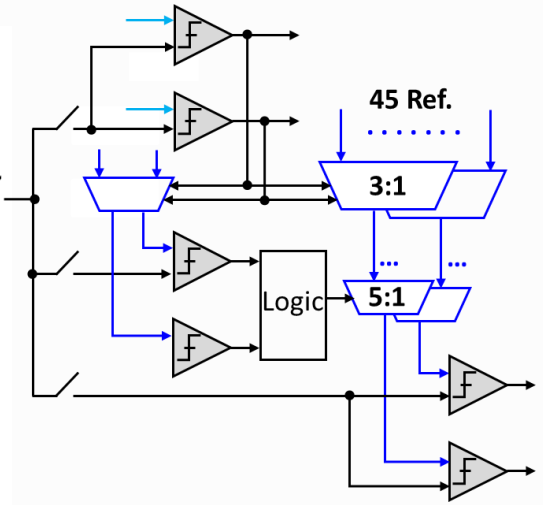




- Edge comparator output defines the next probable location of references

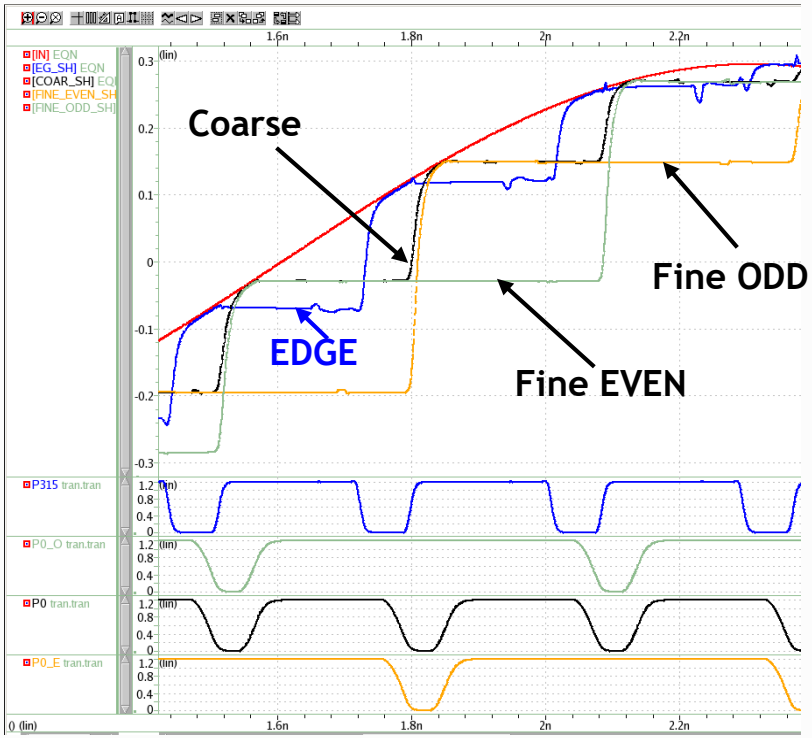
Variable Resolution ADC – 25 dB loss





- Fine references are carried over to the mid of two coarse references

Variable Resolution ADC - Sample and Hold

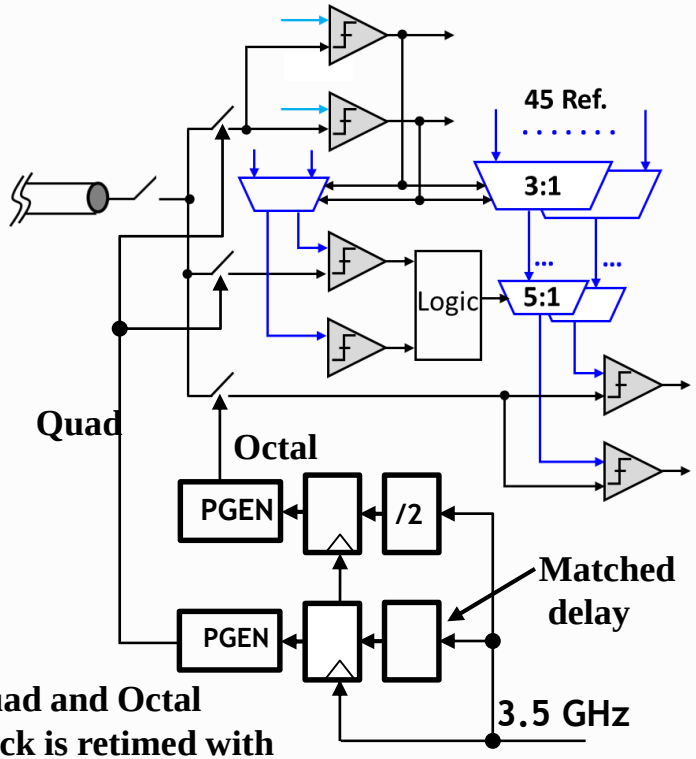


Quad Edge

Octal ODD

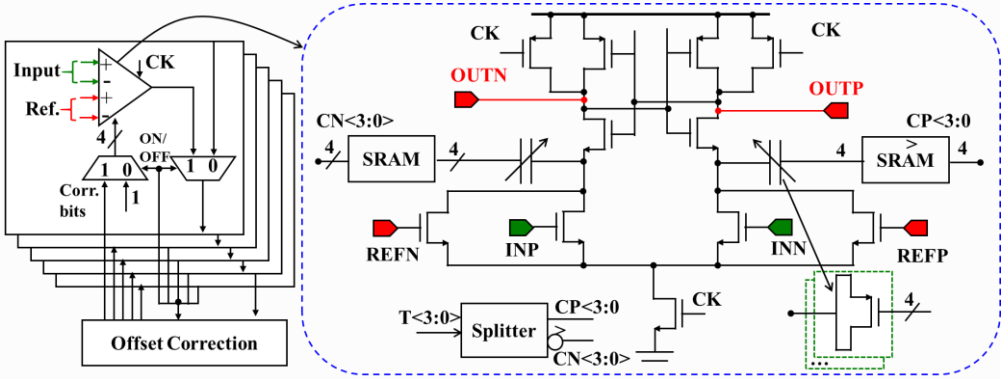
Quad Coarse

Octal EVEN

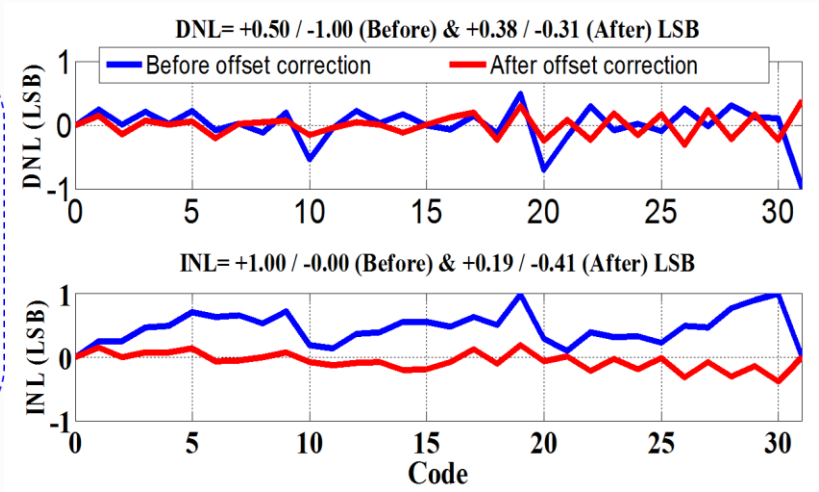


- **Quad and Octal clock is retimed with a the original quad clock**

ADC Offset Correction

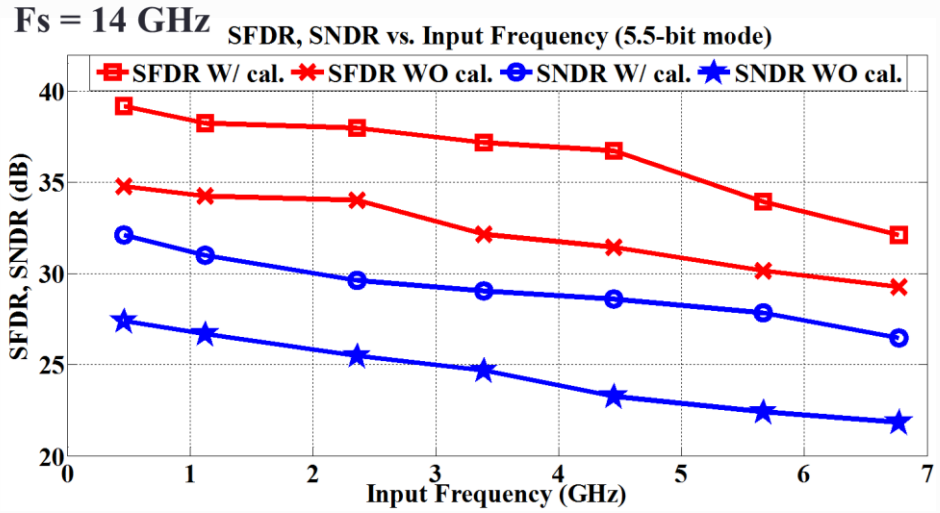


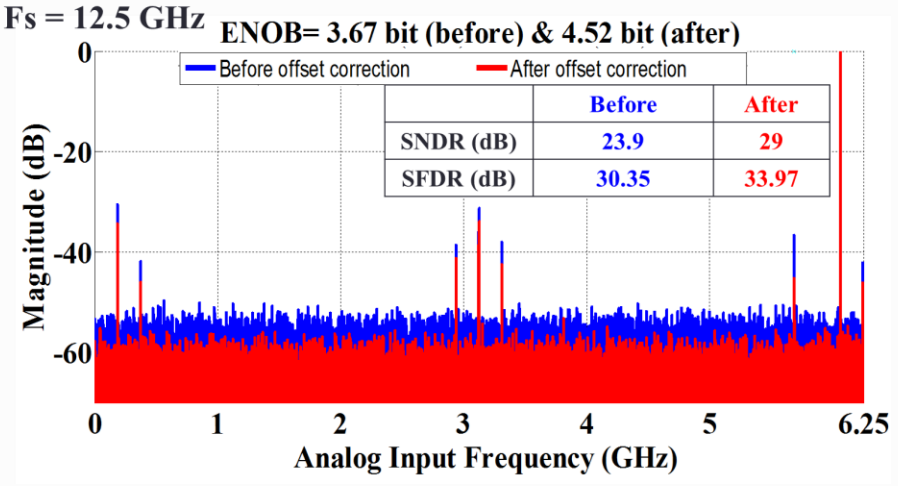
Ref: [2]



- **Unbalance the capacitive load attached to the input of the strong-ARM latch**
- **Store the bit-decisions into a 6T SRAM to reduce the area.**

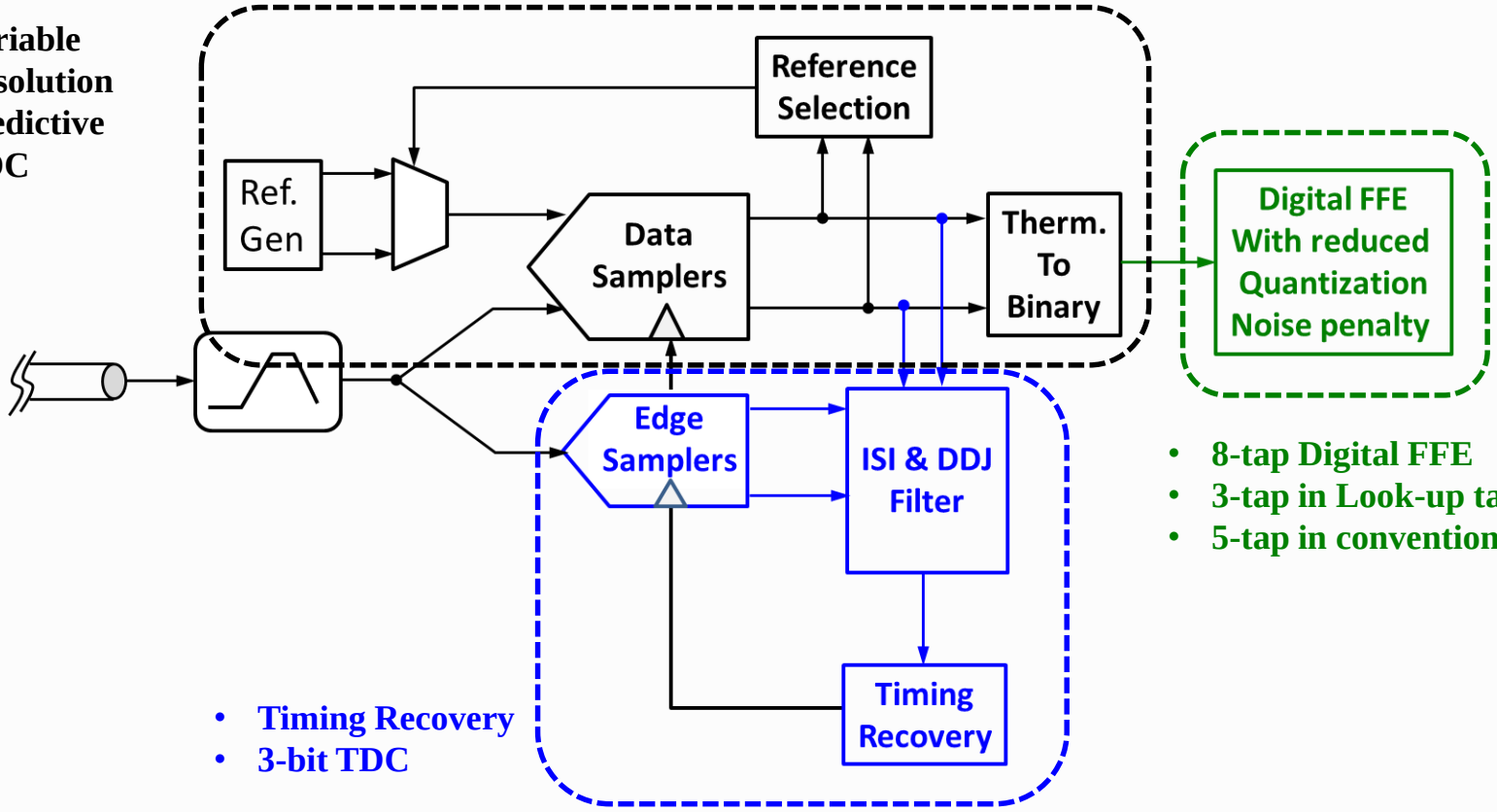
Measured ADC Performance





PAM-4 Digital Receiver Architecture

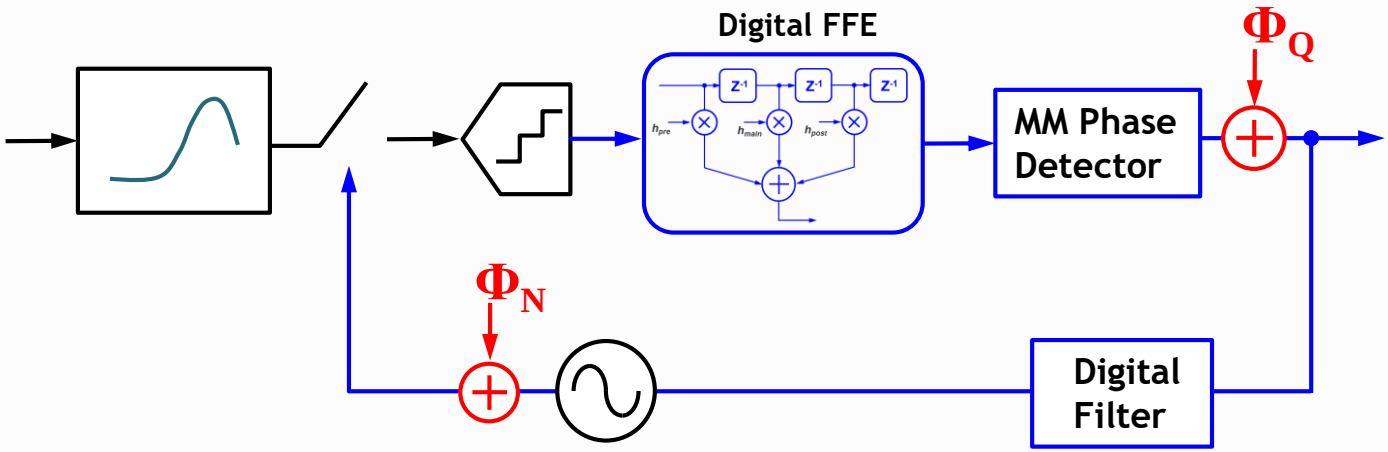
- **Variable Resolution**
- **Predictive ADC**



- **8-tap Digital FFE**
- **3-tap in Look-up table**
- **5-tap in conventional way**

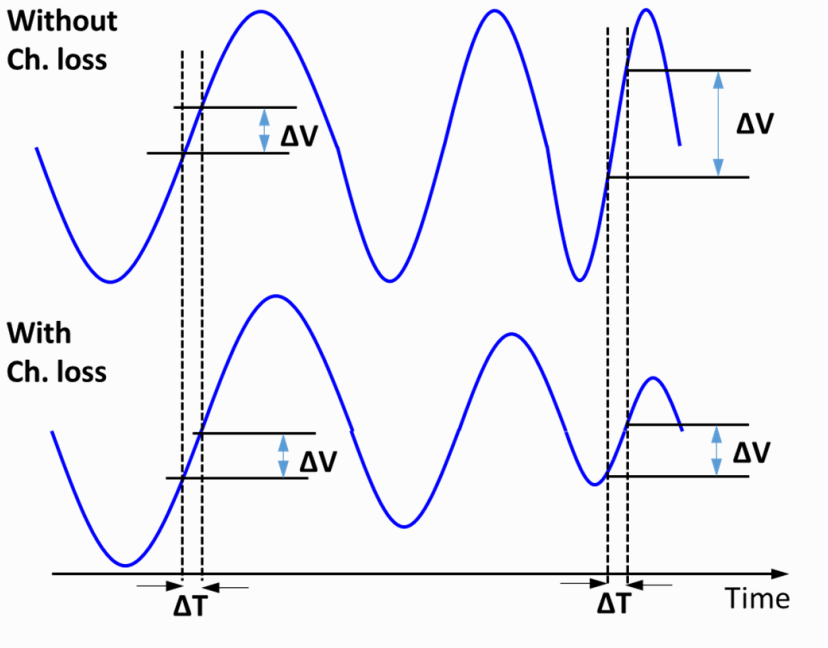
- **Timing Recovery**
- **3-bit TDC**

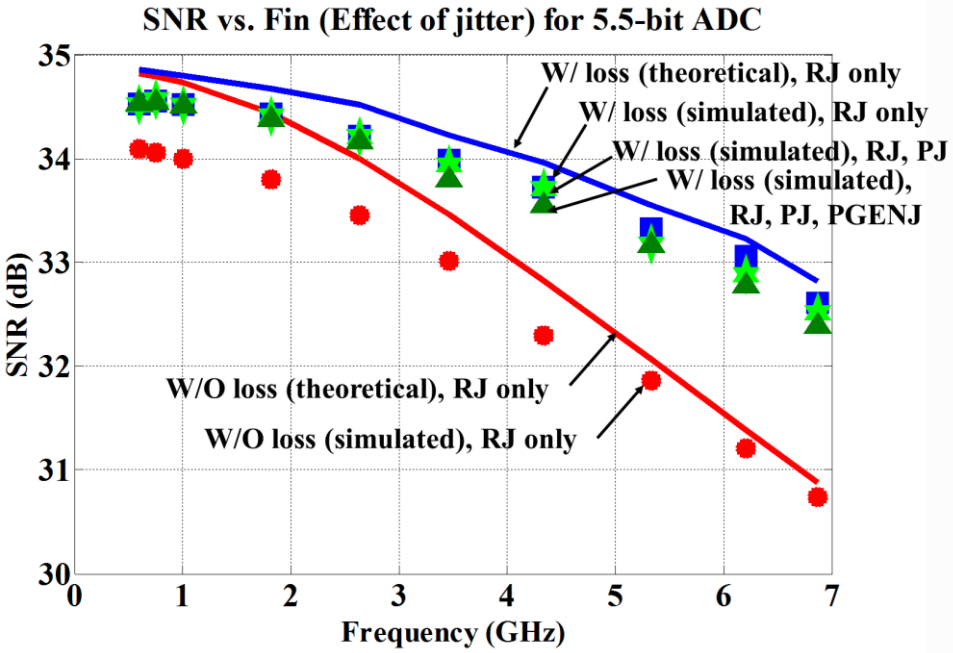
Timing Recovery Challenge for ADC-based Receiver



- MM based phase detection is not as robust as 2x (i.e. data and edge) sampled CDR
- Bang-bang or 1 bit phase quantization at the Phase detector increases in-band jitter
- Lowering loop bandwidth increases VCO phase noise contribution
- Loop latency makes it difficult to achieve wider loop bandwidth

Effect of Timing Noise on SNR

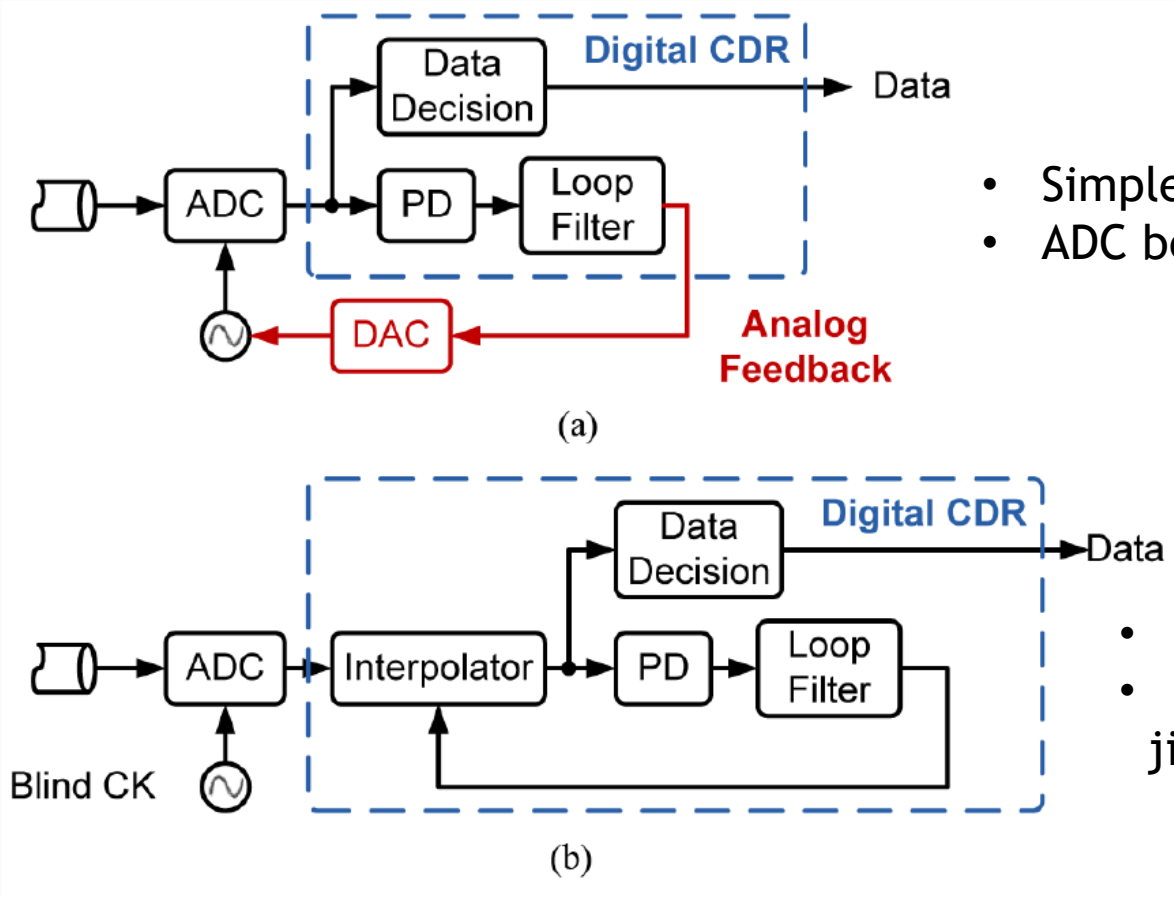




Effect of timing noise on SNR is less when we consider channel loss!!!

Phase Tracking vs Blind ADC based

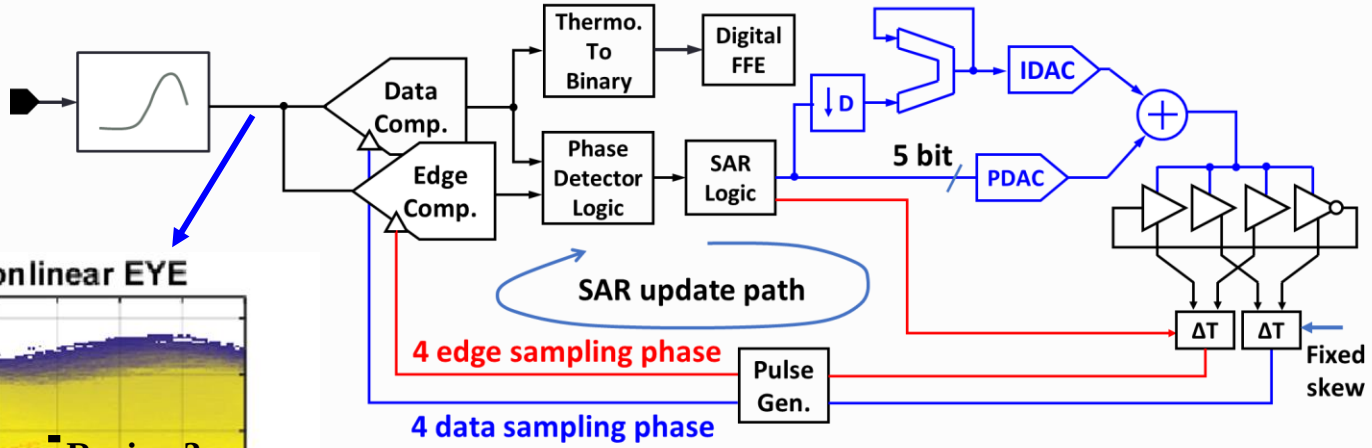
[Clifford *et.al*. JSSC, 2013]

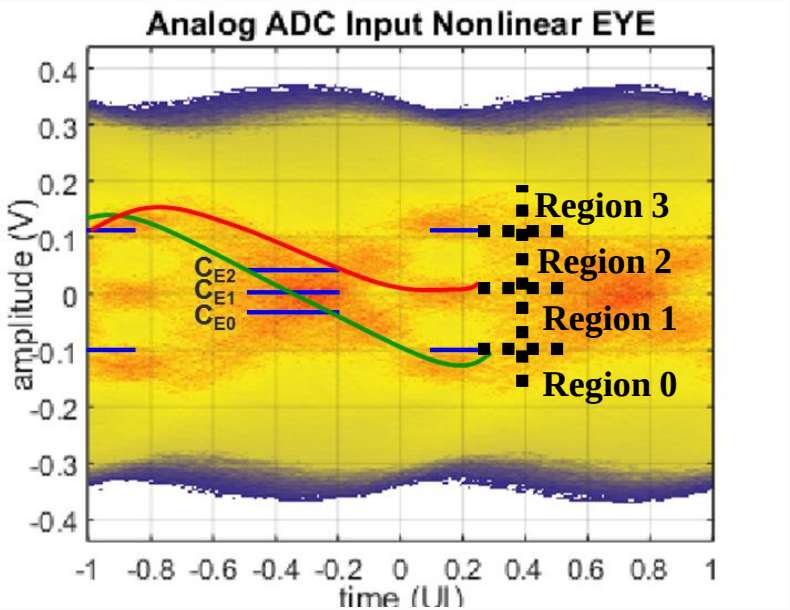


- Simple But latency sensitive
- ADC benefits from jitter tracking

- Less latency sensitive
- ADC does not benefits from jitter tracking

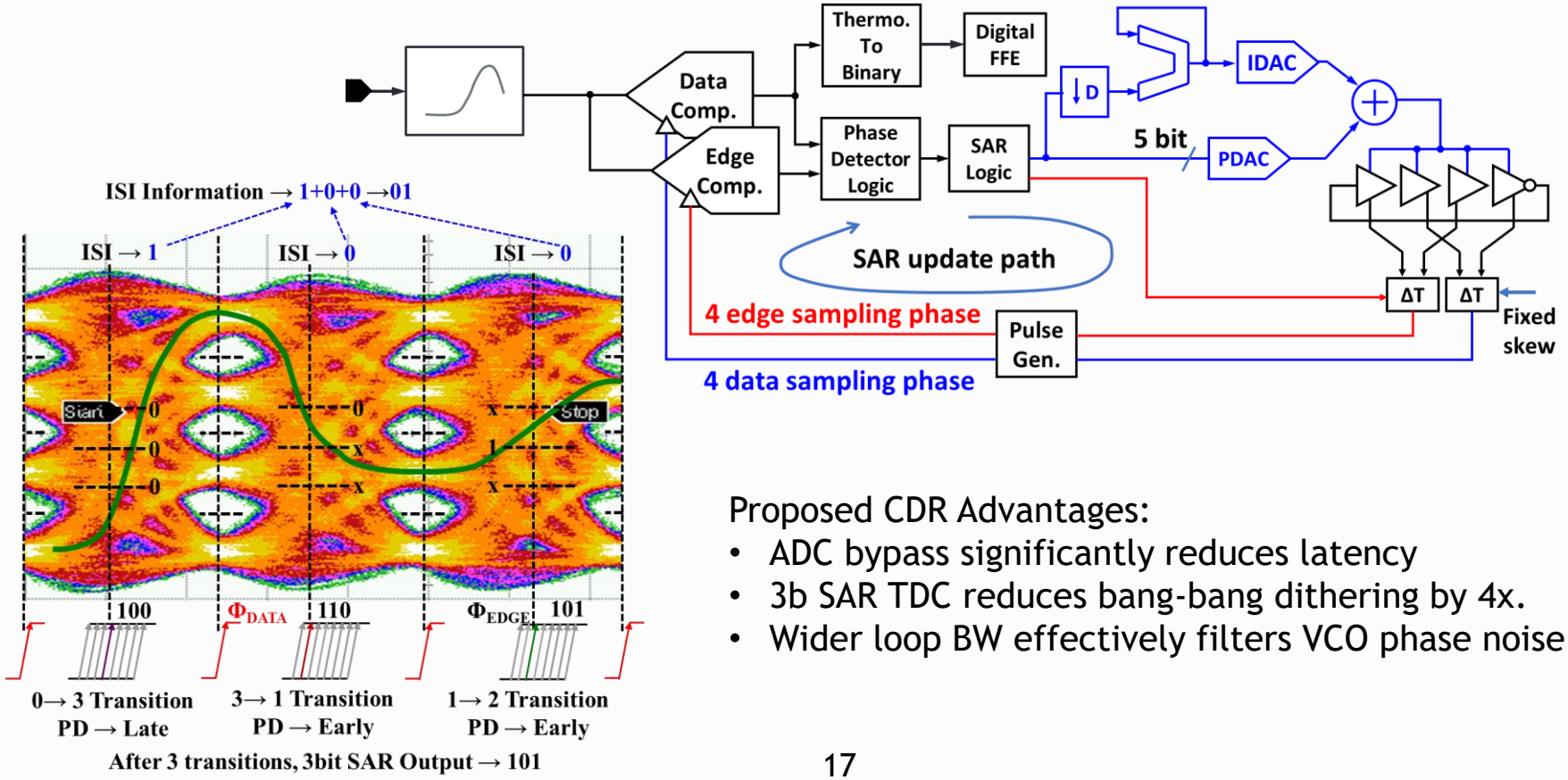
Low-latency Timing Recovery





Transition	C_{E2}	C_{E1}	C_{E0}	PD Output	ISI Info
3→0	0	0	0	0	1
	0	0	1	0	0
	0	1	1	1	0
	1	1	1	1	1
2→0	x	x	0	0	0
			1	1	0
3→1	0	x	x	0	0
	1			1	0
2→1	x	0	x	0	0
		1		1	0

Low-latency Timing Recovery - SAR TDC operation

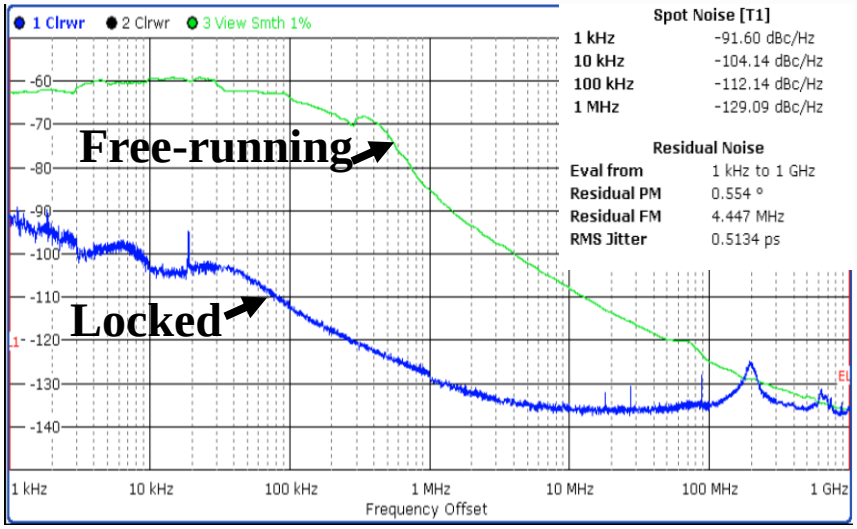


Proposed CDR Advantages:

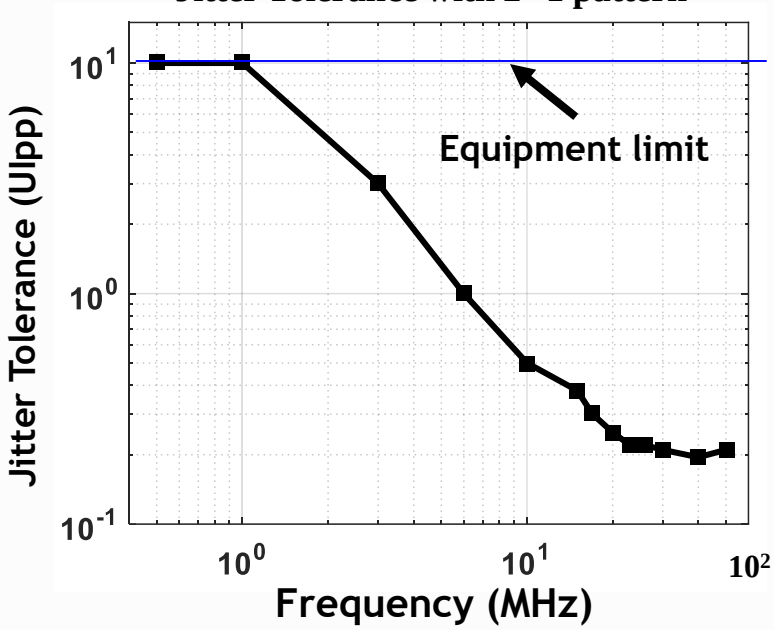
- ADC bypass significantly reduces latency
- 3b SAR TDC reduces bang-bang dithering by 4x.
- Wider loop BW effectively filters VCO phase noise

CDR Performance

Phase Noise



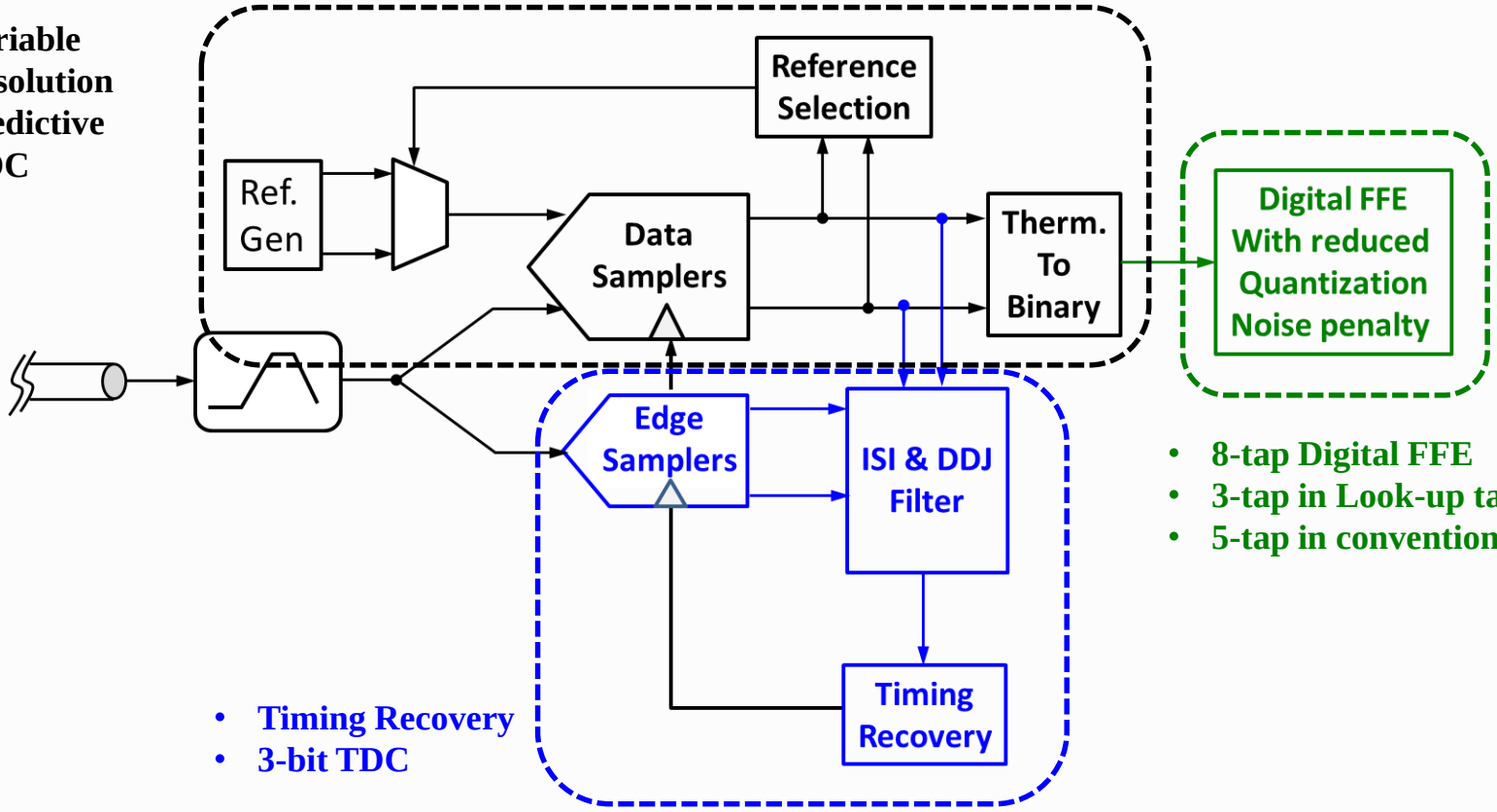
Jitter Tolerance with 2^7-1 pattern



- **Integrated jitter = 0.5 ps**
- **In-band phase noise = - 90 dBc/Hz**

PAM-4 Digital Receiver Architecture

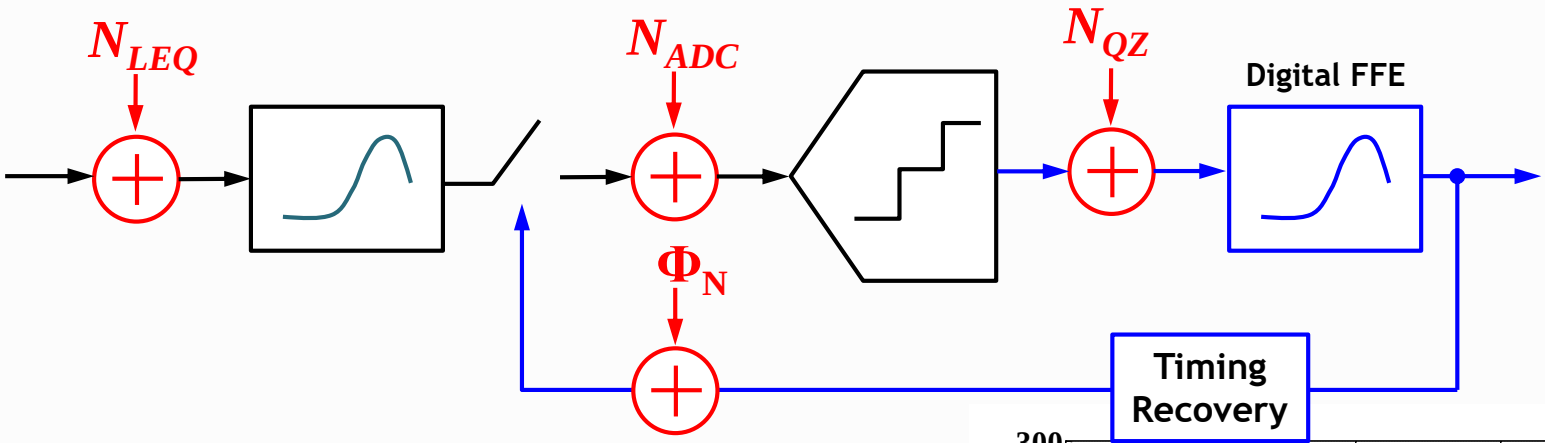
- **Variable Resolution**
- **Predictive ADC**



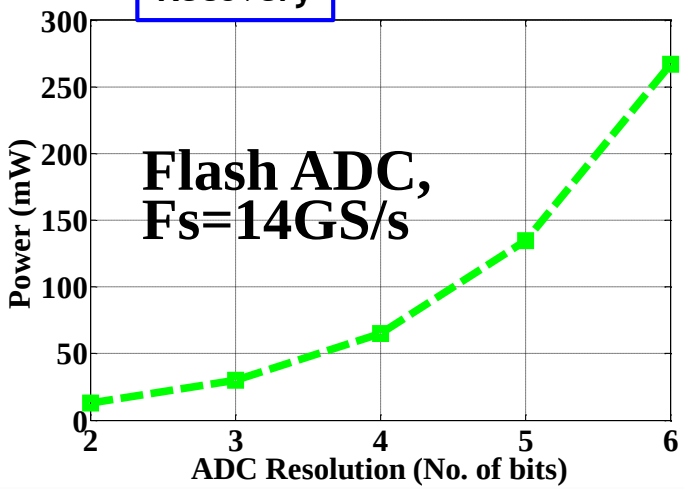
- **8-tap Digital FFE**
- **3-tap in Look-up table**
- **5-tap in conventional way**

- **Timing Recovery**
- **3-bit TDC**

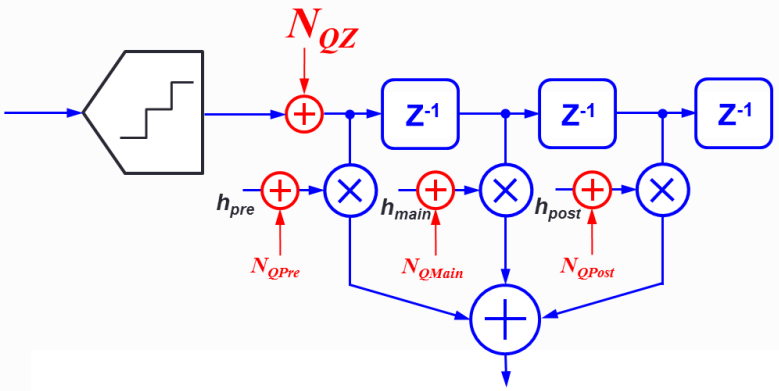
Noise Sources in ADC-based Receiver



Noise Source	Constrain	Transfer Gain
N_{LEQ}	Power/Gain/BW	LEQ + FFE
Φ_N	Power and latency	FFE
N_{ADC}	Power/Settling time	FFE
N_{QZ}	ADC Resolution	FFE

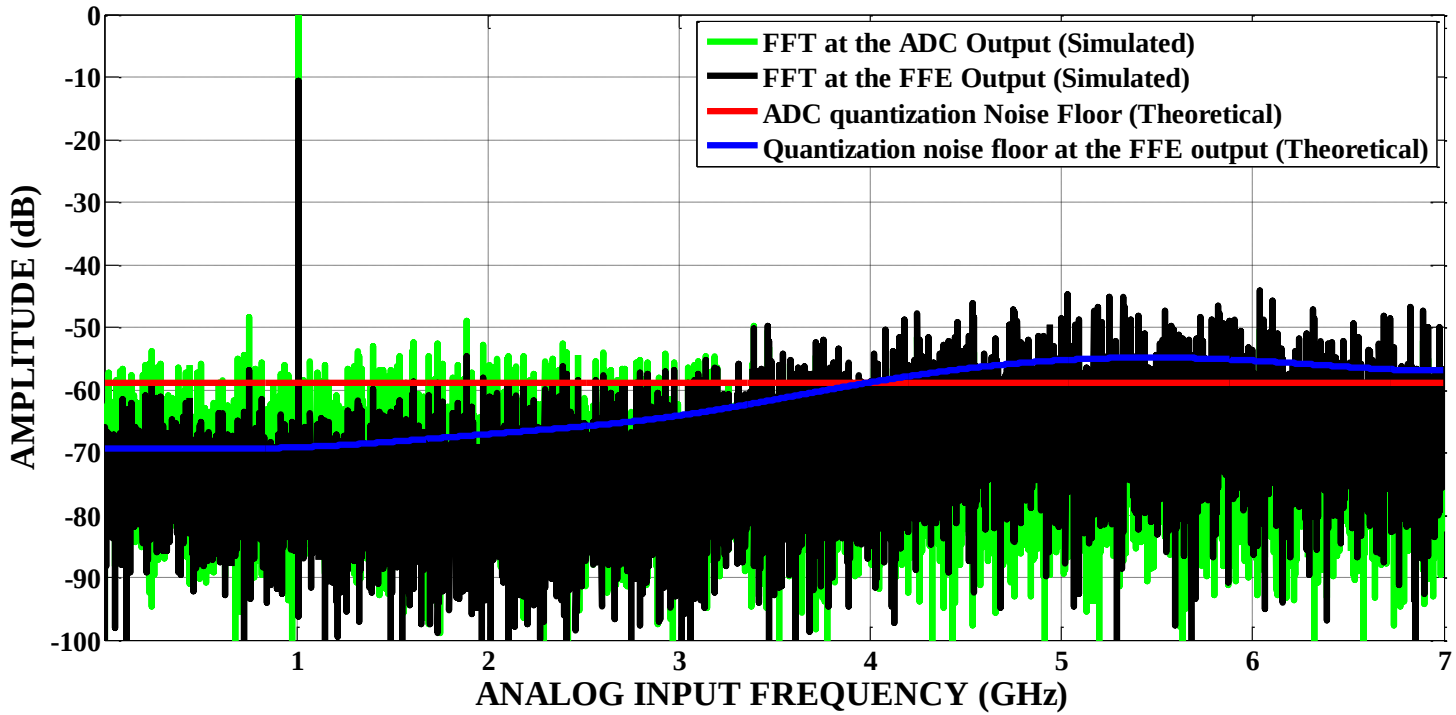


Quantization Noise Impact

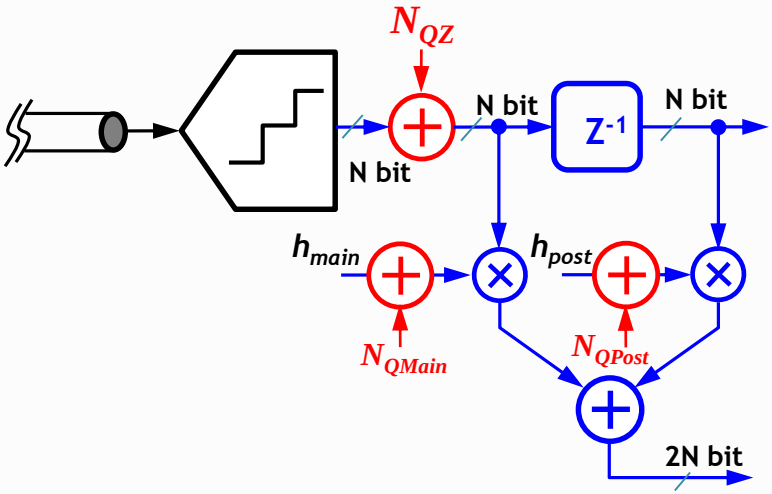


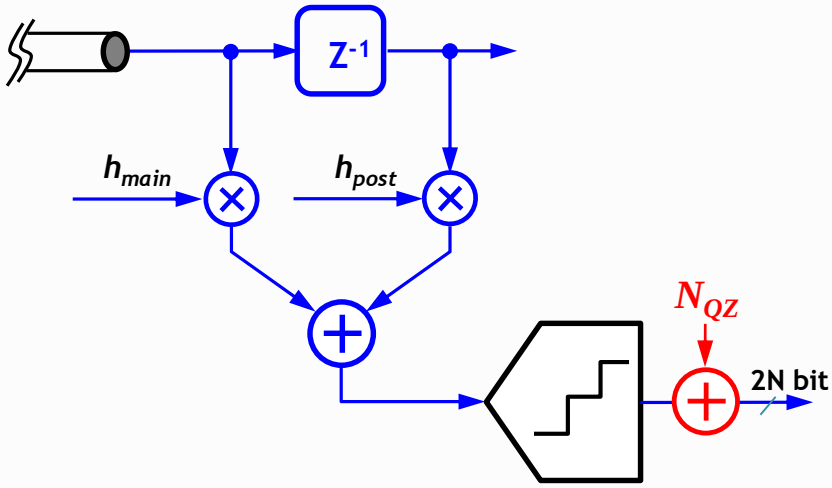
$$N_{QZ,out} = N_{QZ} \cdot |h_{FFE}|^2 + \sqrt{\frac{N^2_{QPre} W^2_{Pre} + N^2_{QMain} W^2_{Main} + N^2_{QPost} W^2_{Post}}{3}}$$

$$W_X = \frac{h_X}{h_{pre} + h_{main} + h_{post}} \quad , x = Pre, Main, Post$$



How to reduce ADC quantization noise impact?



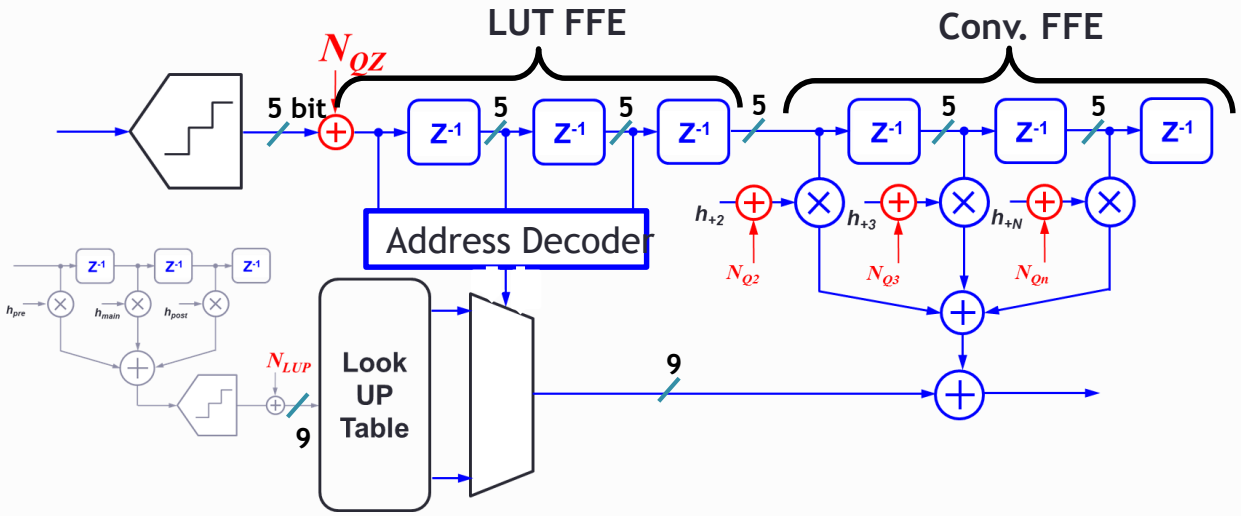


Although Digital FFE output can be 2N bit, we are we are still limited by ADC's N bit resolution

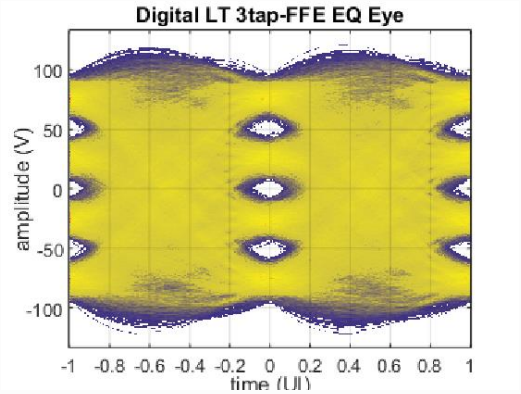
If FFE can be moved ahead of the ADC than we can Minimize ADC's quantization noise penalty

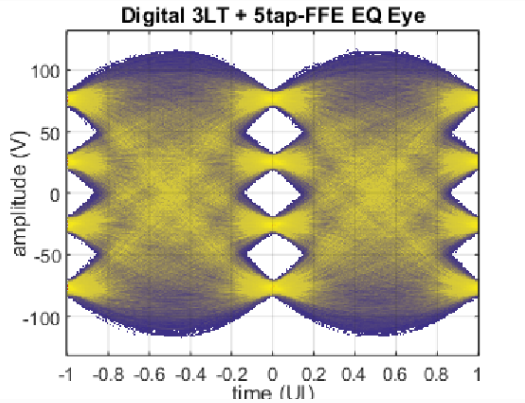
How can we build a digital FFE with resolution better than the ADC?

Reducing Quantization Noise Impact



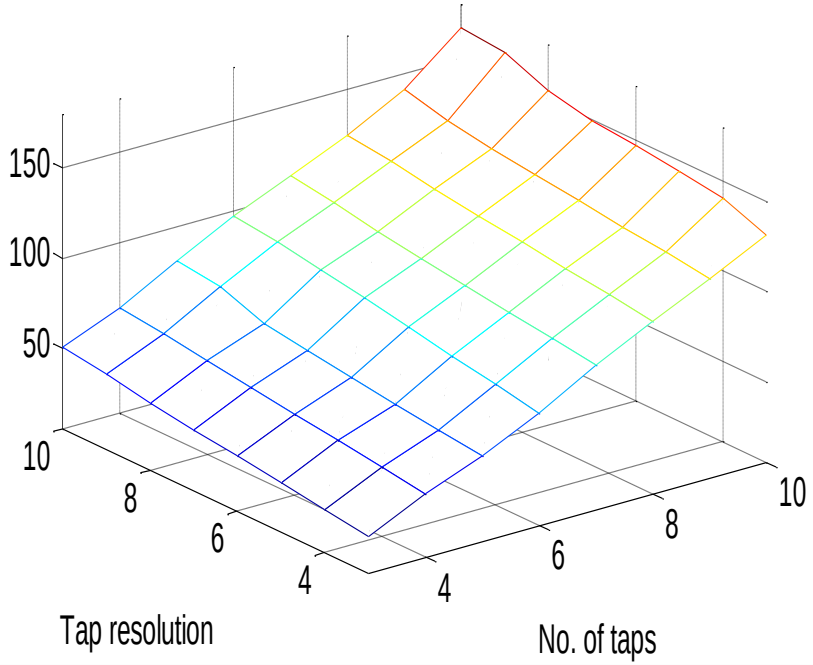
- LUT based first three taps reduces quantization noise impact
- 3 to 8 taps does not significantly amplify quantization noise



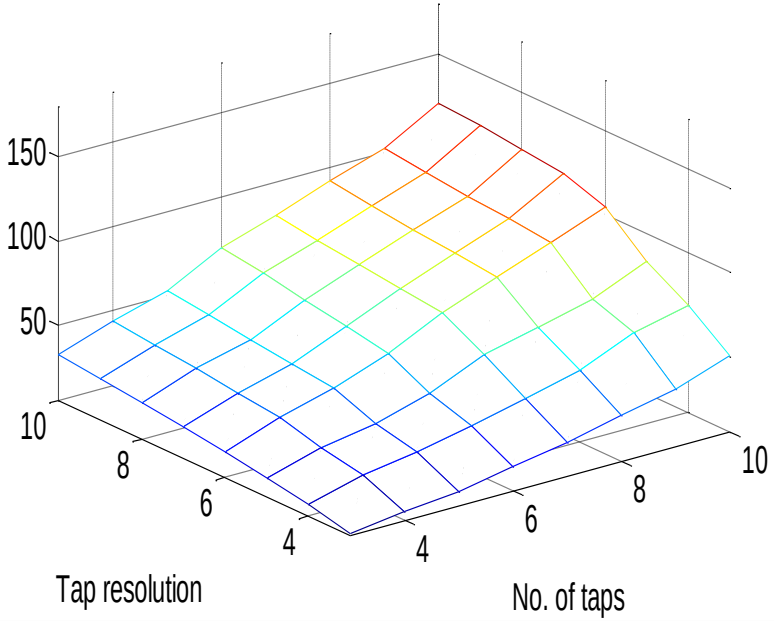


Reducing Quantization Noise Impact

8-tap Conventional



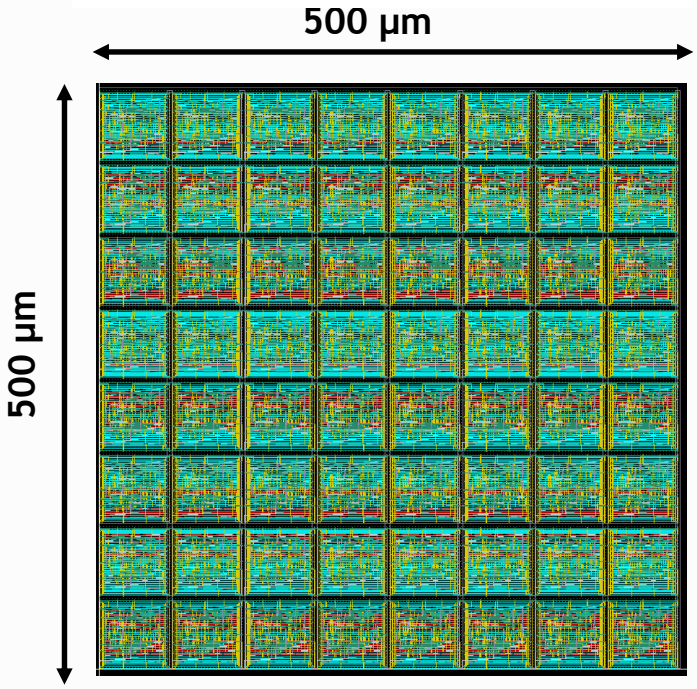
3-tap LUT + 5-tap Conventional



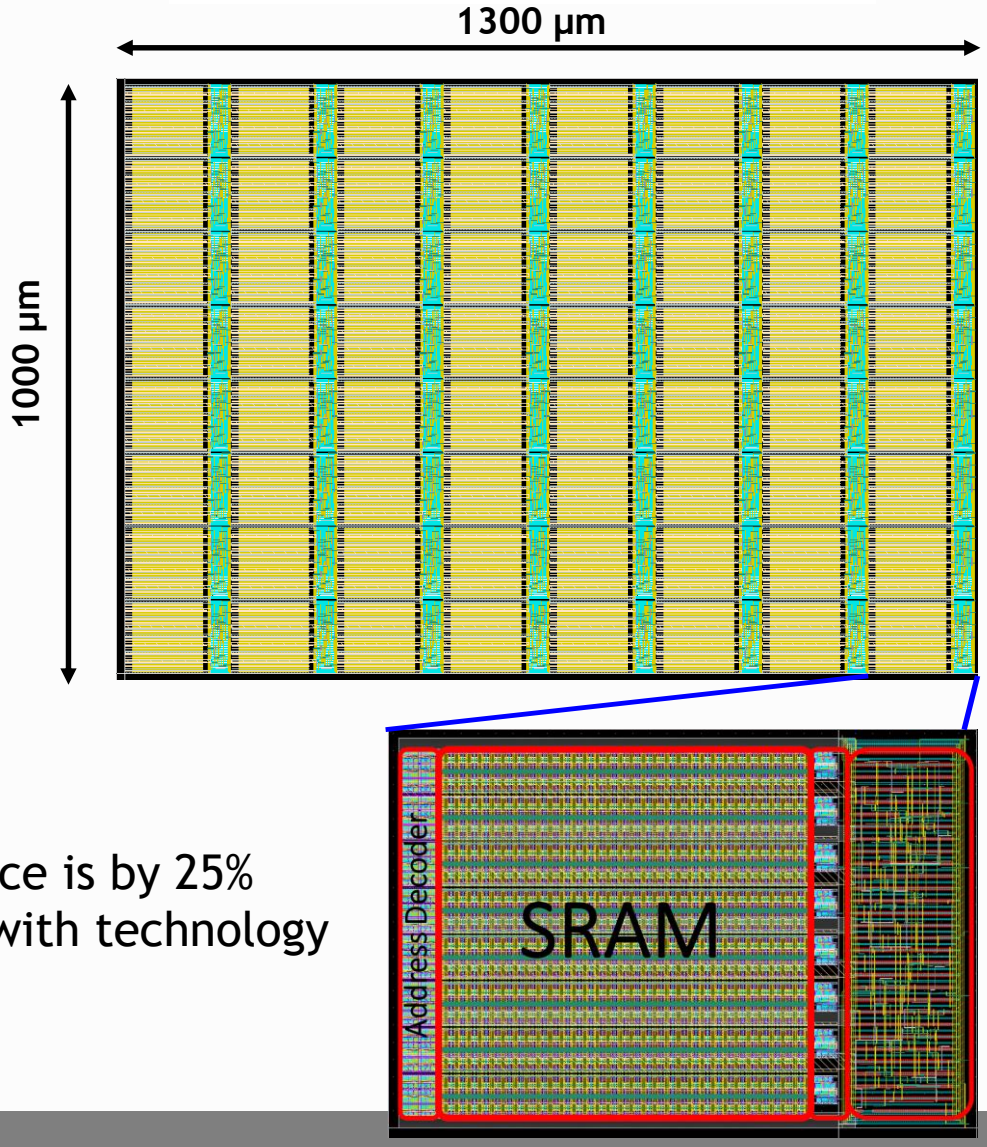
Proposed approach is 30% lower power compared to conv. FIR implementation

Area Impact of the proposed solution

8-tap Conventional

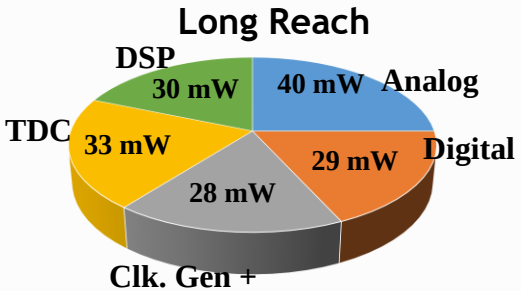


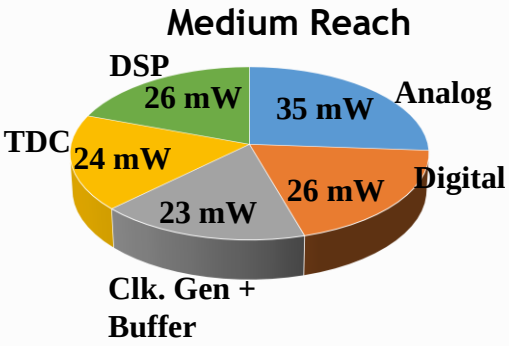
3-tap LUT + 5-tap Conventional



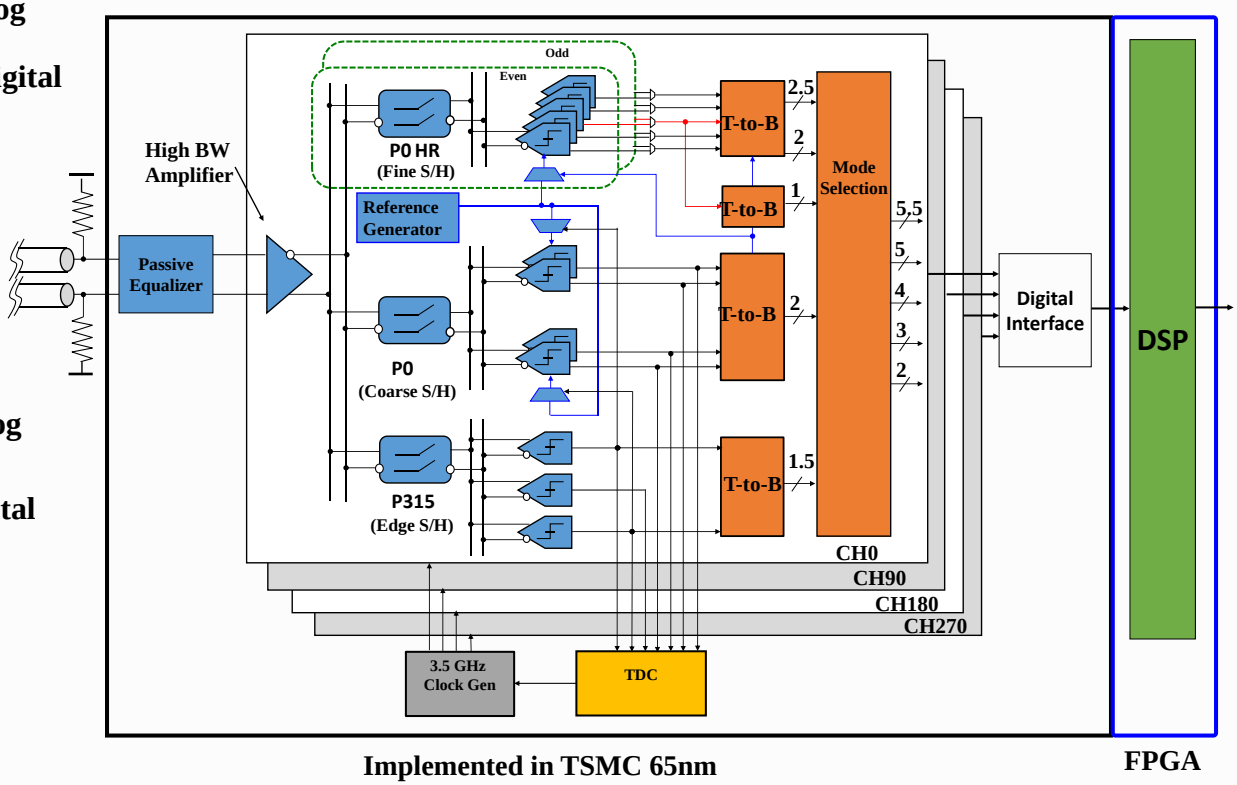
- Area increases by 4x but
  - Standard cell SRAM will reduce is by 25%
  - Area will scale significantly with technology

Implemented Prototype in 65nm CMOS

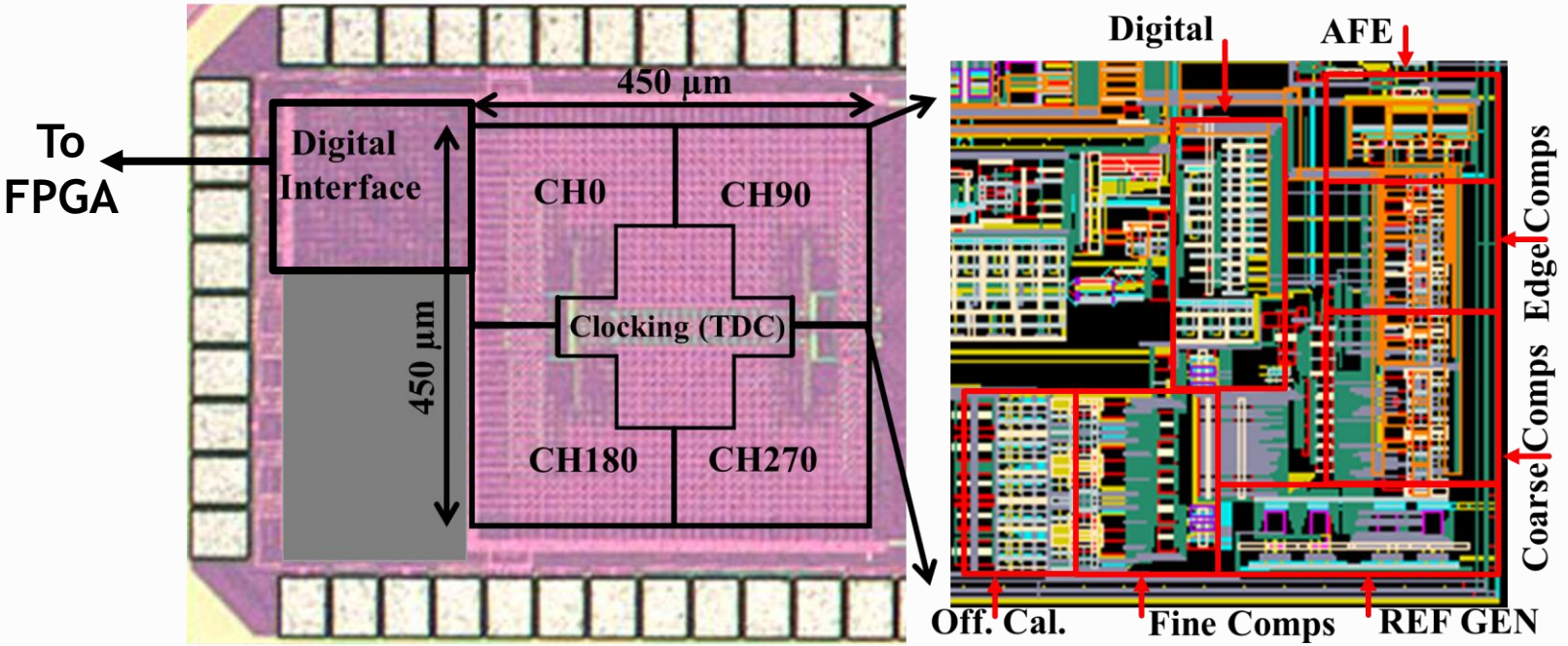




Digital:
- T-to-B, Mode selection
- Retimer

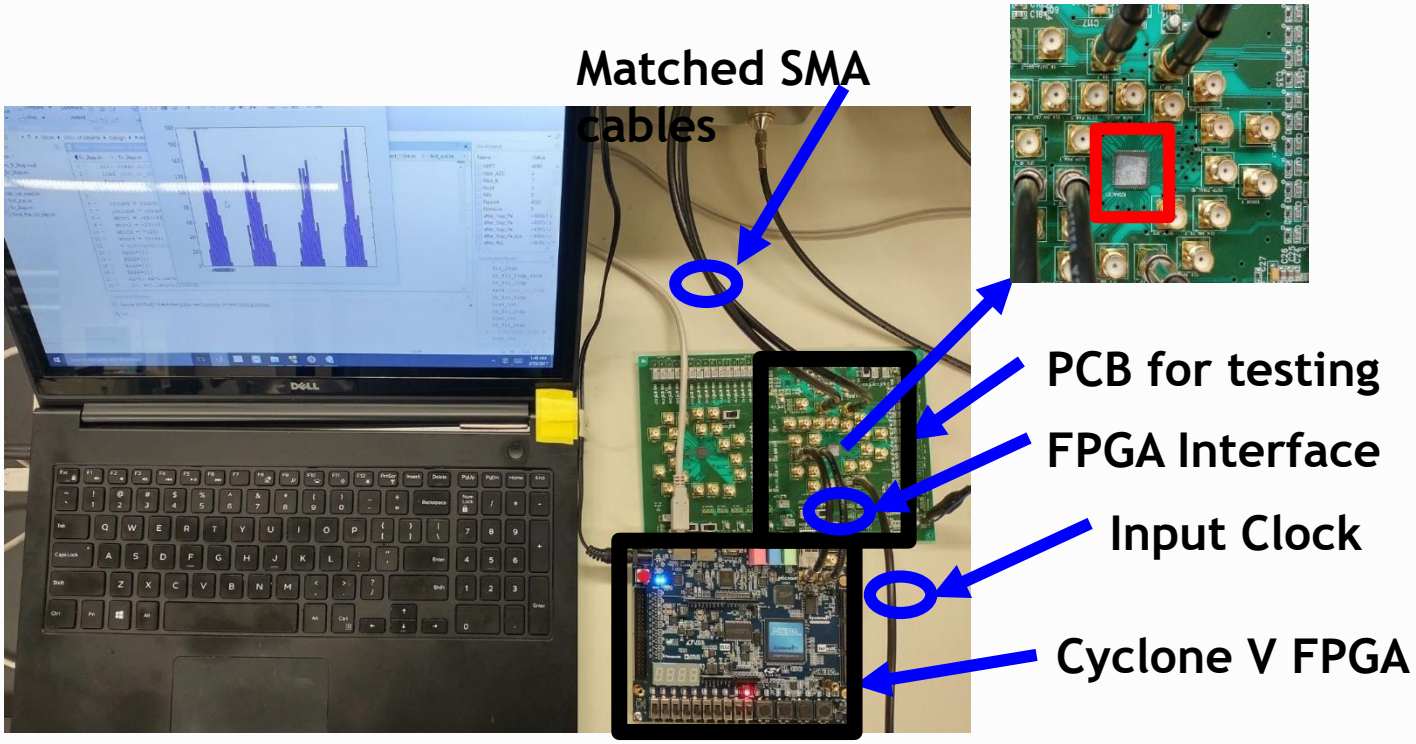


Implemented Prototype in 65nm CMOS



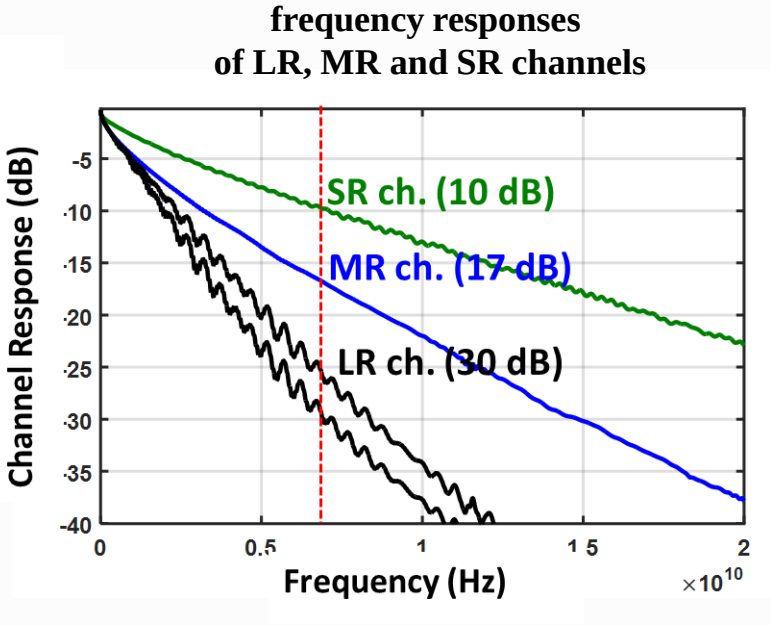
- **Heavily digital solution**
- **Input needs only 7 GHz bandwidth**

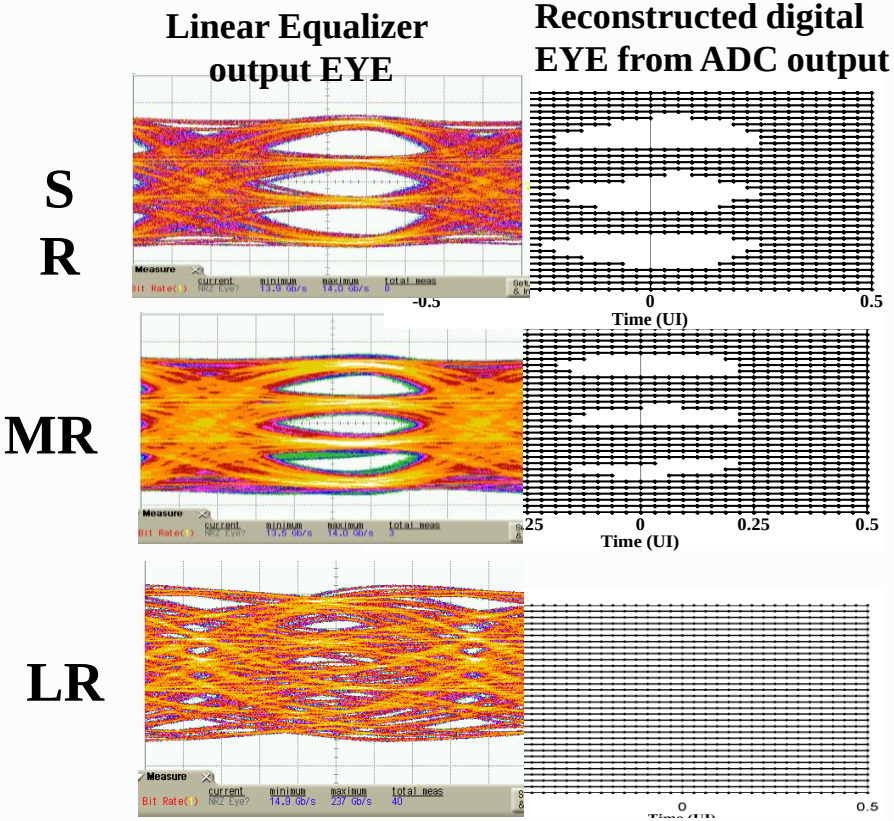
Experimental Setup



- **Varying channel loss by cascading SMA cables.**

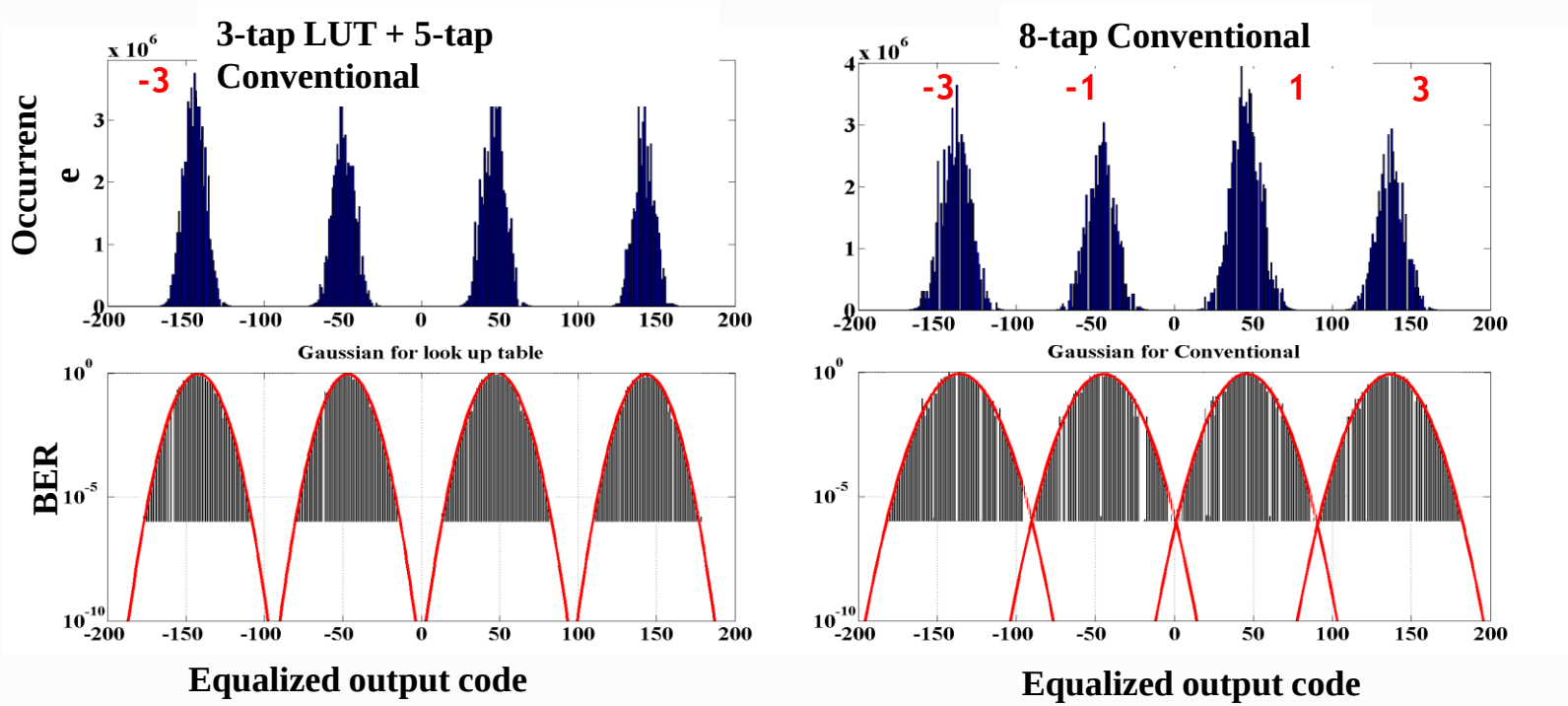
Input EYE in Digital Domain





- Tx has 6 dB equalization
- Linear equalizer boost: 6 to 14 dB

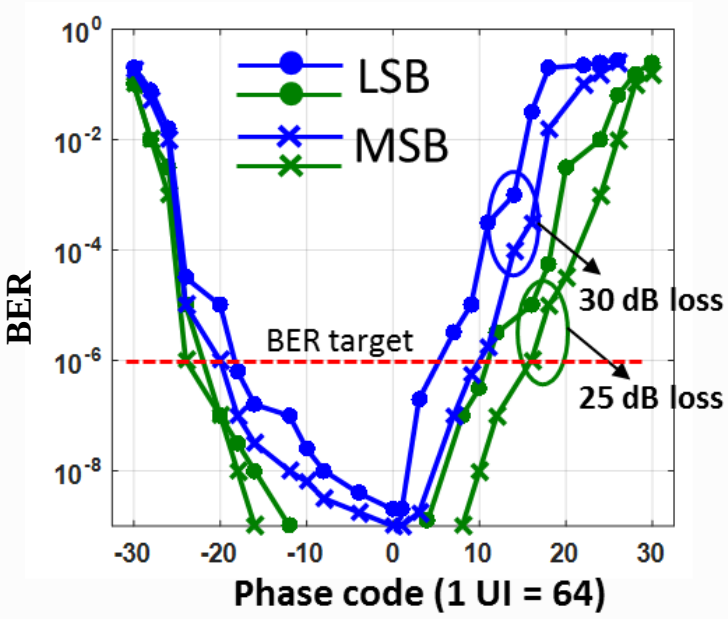
Link Margin at 28Gb/s 30 dB Channel

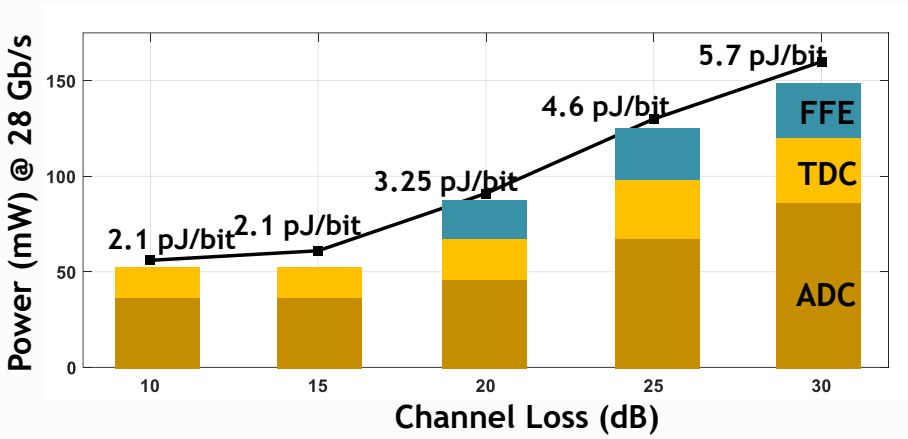


- FPGA gives the distribution of the bins
- The distribution is converted into log-scale
- Gaussian fit to extract the BER.

Link Margin Test and Energy Efficiency

Data rate: 28 Gb/s PAM-4





- **Receiver can achieve BER up to 10^{-9}**

Comparison with state-of-art

	Shafik ISSCC 2015[4]	Frans VLSI 2016[5]	Cui ISSCC 2016[3]	Rylov ISSCC 2016 [6]	**This Work**
Technology	65 nm CMOS	16 nm FinFET	28 nm CMOS	32 nm CMOS	**65 nm CMOS**
Data Rate (Gb/s)	10 NRZ	56 PAM-4	32 PAM-4	25 NRZ	**28 PAM-4**
ADC Architecture	32x TI SAR ADC	32x TI SAR ADC	32x TI SAR ADC	4x Flash ADC	**4x Flash ADC**
ENOB@ Nyquist	4.74	4.9	5.85	4	**4.1**
Timing Recovery	N/A	Baud-rate	Baud-rate	Baud-rate	**Edge & Data Sampled**
Tracking BW	---	---	---	---	**10+ MHz**
Jitter Tolerance	---	----	---	---	**0.2 UIpp @ 50 MHz**
Channel Loss Equalization	36.4 dB @ 5 GHz	25 dB @ 14 GHz	32 dB @ 8 GHz	40 dB @ 12 GHz	**30 dB @ 7 GHz**
Power (mW)	79(w/o DSP) 87(w DSP)	410(w/o DSP)	320	453	**130@30 dB, 45 @ 15 dB — w/o DSP; 160@30 dB, 60 @ 15 dB — with DSP**
FOM (pJ/bit)	8.7	7.32	10	18.12	**5.71@ 30 dB, 2.14@ 15 dB — with DSP**

Summary of ADC Based Receiver

- ADC- DSP Based receivers are the future for multilevel signaling in advanced CMOS – but it's power has to be reduced.
- DSP needs to be more information efficient – Non-uniform quantization is a simple way to improve effective resolution.
- ADC for wireline is different than general purpose ADC. General purpose ADC considers each sample 'uncorrelated' but in reality channel ISI makes them 'correlated' – predictive ADC is a simple way to take advantage of that.
- Timing recovery is as important as data recovery – Multibit TDC and lower latency is an effective way to improve timing recovery loop and meet jitter requirement of the ADC.